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LB-946

FACTORS IN THE DESIGN OF KEYED CLAMPING CIRCUITS

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Approved

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Introduction

In the various signal processing operations performed in the generation of the color television signal, it is sometimes necessary that the signals being processed possess their d-c component, and further be set at some definite d-c reference level. Keyed clamping circuits are usually employed to satisfy these requirements, and are commonly used for this purpose in such apparatus as linearity correcting amplifiers, color-plexers, encoders, and stabilizing amplifiers.

Several forms of keyed clamping circuits can be used. These include single, double, and quadruple diode types, as well as various triode types.[1] At present however, the most commonly employed clamp circuit is the double diode type, referenced against some fixed potential. The analysis to be made in the present bulletin is principally concerned with this particular circuit, but many of the results are applicable to the other forms of clamps.

Circuit Description

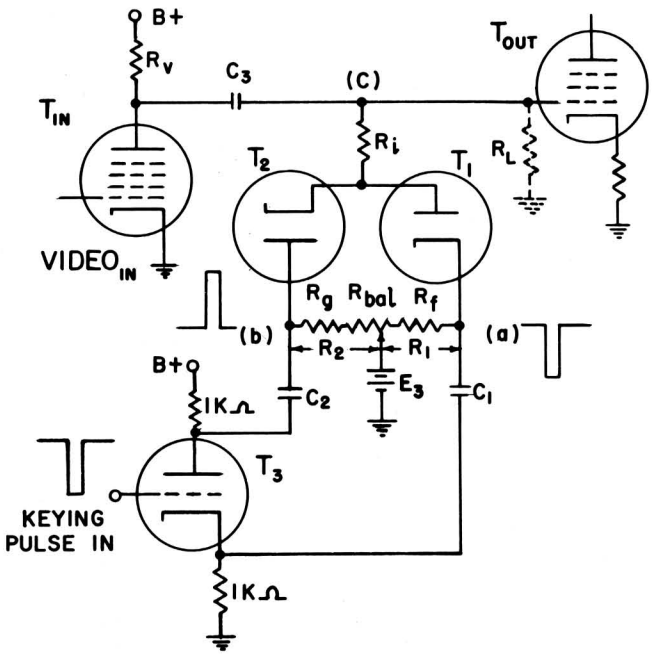
Fig. 1a shows a typical keyed double diode clamping circuit as applied to a video amplifier chain. The video signal to be clamped, such as that of Fig. 1b, appears at the plate of the amplifier T_{in}. This signal has lost its d-c component as can be deduced from the fact that its blanking level is not constant, but rather varies as a function of the video content in the signal. The clamping operation usually takes place during the latter part of the horizontal blanking period. At that time the clamping circuit is keyed on, and in effect "looks" at the video signal to see if its blanking level is constant and at a prescribed voltage. If it is not, the circuit operates to correct the situation, so that the video signal, at the grid of T_{out}, will appear as in Fig. 1c.

The clamping circuit itself forms the grid return for T_{out} and consists of the circuitry associated with the diodes T_1 and T_2 and the triode driver T_3. A resistor R_i is commonly included in the circuit to help prevent the higher frequency components of the clamp keying pulses from appearing in the video signal on the grid of T_{out}. The diodes are connected in a bridge configuration. The lower arms of the bridge consist of fixed resistors R_f and R_g, and a balancing potentiometer R_{bal}. The tap on R_{bal} is tied to the reference voltage E_3. The total resistance from this tap to point (b), the plate of T_2, is labeled R_2, and the total resistance from the tap to point (a), the cathode of T_1 is labeled R_1.

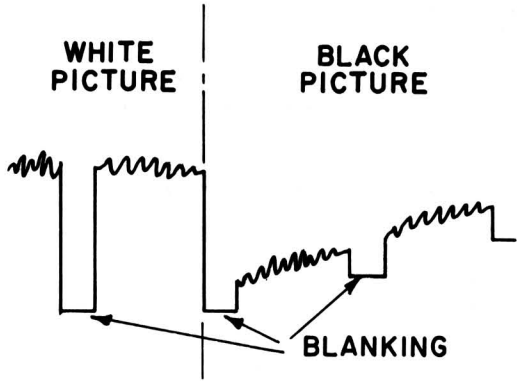
[1] *LB-745, The Television DC Component.*

Clamping Operation

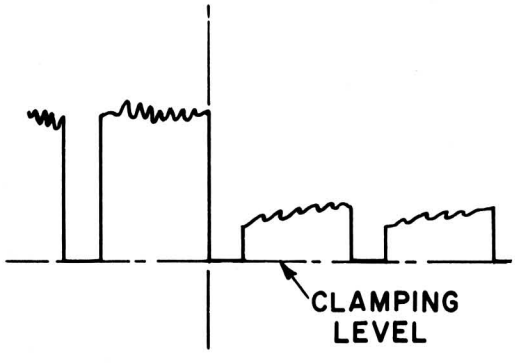
During the clamping interval a negative pulse is applied to the grid of the driver tube T_3 so that positive and negative going pulses appear across its plate and cathode loads respectively. These are the clamp keying pulses. They are applied to the diodes causing them to conduct through the capacitors C_1 and C_2.



(a) Keyed clamping circuit.



(b) Video input.



(c) Video output.

Fig. 1 – Keyed clamping operation.

Consequently, during the clamping interval, electrons leave the upper plate of C_1, charging it in the positive direction, pass through the diodes and enter the upper plate of C_2, charging it negative. This action develops a back bia voltage, approximately equal to the peak of the clamp pulses, across each of the capacitor-resistor combinations C_1R_1 and C_2R_2 of proper polarity to prevent diode conduction during the video interval.

The operation of the circuit when R_1 equals R_2, and the amplitudes of the keying pulses are equal, can be seen by considering what happens when a video signal which has lost its d-c component, such as that of Fig. 1b, appears at the plate of T_{in}. As long as th blanking level of this signal is constant, the voltage during the clamping interval at the junction point (c) on Fig. 1a remains the same as that of the reference voltage E_3. Consequently, no charge flows into C_3, and any electrons leaving C_1 flow into C_2. However, when the picture content changes, as shown in Fig. 1b, for example, the black level shifts upward and an unbalance voltage which is more positive than the reference voltage appears at the grid of T_{out} during the clamping interval.

Under these conditions, electrons are transferred from C_1 to C_3 so that the voltage of the blanking signal at the grid of T_{ou} falls toward the reference voltage. If the video signal is such that its blanking level occurs at a voltage which is lower than the reference voltage, electrons are transferred from C_3 to C_2 and the voltage at the grid of T_{out} rises toward the reference voltage. In this manner, a clamping level equal to the reference voltage is maintained, and the d-c component is re-inserted into the video signal, which now appears at the grid of T_{out} as in Fig. 1c. Undesirable low frequency disturbances, such as hum or line bounce, are removed from the video signal by this same mechanism.

Clamp Level

It is usually necessary to set the clamping level at some specific voltage. This can be done by setting the reference voltage E_3 at the desired voltage, as discussed in the precedin section. However, the level can also be set by varying the relative sizes of R_1 and R_2 by means of a potentiometer such as R_{bal} of Fig. 1.

In this latter case the level setting takes place as follows: when the two diodes conduct during the clamping interval, the tw

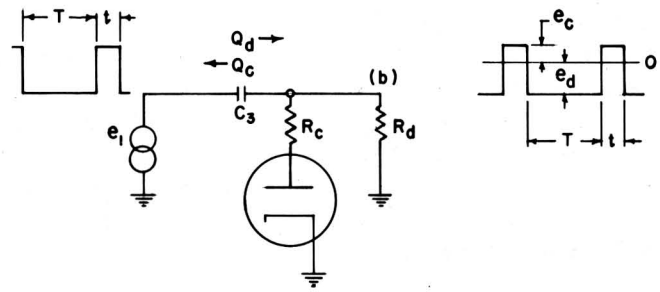
capacitors charge in series, so that the electron charge is the same for both. Consequently under equilibrium conditions they must each discharge an equal number of electrons through R_1 and R_2. If the two discharge resistors are equal, the voltage developed across them will be equal and opposite, and the clamping level will be equal to the reference voltage. However, when R_{bal} is adjusted so that R_1 and R_2 are not equal, the voltage across each of them will be proportional to their resistance. For example, if the tap on R_{bal} is moved to the left, R_2 decreases and R_1 increases, thereby making point (a) more positive and point (b) less negative. Consequently, the potential of the entire bridge circuit, and the resultant clamp level, is moved in the positive direction.

Effects of Leakage

The preceding analysis assumed that the resistance looking into the complete circuit from point (c) on Fig. 1a was substantially infinite. However, under certain operating conditions, such as when there is leakage across the diodes or C_s, or when gas current or grid emission occurs in T_{out}, the resistance looking into the circuit from (c) may be reduced sufficiently to affect the d-c level set by the clamp. This leakage resistance, labeled R_L, is drawn dotted in Fig. 1a, and for purposes of analysis is shown returned to ground. Its value is usually not stable, but rather varies as a function of such things as ambient temperature and humidity, equipment warm-up conditions and other factors. Consequently it must be given due consideration in circuits where a high degree of stability of clamp level is required. In order to evaluate this effect, as well as some of the others which contribute to the stability problem, a more comprehensive analysis of the circuit is required. The analysis to be presented, while not completely rigorous, yields results that are generally applicable within the limits of operating conditions usually encountered in television systems. It is based on conservation of the charge on the three capacitors involved in the circuit, and as examples of the method consider the cases of two somewhat simpler but closely related circuits: the d-c restorer, and the pulse peak detector.

DC Restorer

Fig. 2 shows a d-c restorer operating on a train of narrow pulses[2]. The restorer is idealized to the extent that all the resistance in the charge path of the coupling capacitor C_s is placed in series with the diode. If it is assumed further that the charging time constant R_cC_s is long compared to the pulse-on period t and the discharge time constant R_dC_s is long compared to the pulse-off period T, and that t is much smaller than T, the d-c restored pulses appear at the point (b) as shown. The problem is to determine the amount by which the peaks of the pulses overshoot the reference potential,



$$Q_c = \frac{e_c}{R_c} t \qquad Q_d = \frac{e_d}{R_d} T$$

BUT AT EQUILIBRIUM

$$Q_c = Q_d$$

$$\therefore \frac{e_c}{e_d} = \frac{R_c}{R_d} \times \frac{T}{t}$$

Fig. 2 - D-C restorer.

which in this case is ground. Since restoration takes place with respect to ground, the diode conducts and C_s charges a number of electrons, Q_c, through R_c when the pulse goes above ground. During the rest of the interval the diode is cut off and C_s discharges a number of electrons, Q_d, through R_d. The overshoot required for charging C_s is the voltage labeled e_c and the discharge voltage is labeled e_d. The d-c restorer equation to be developed expresses the relationship between these voltages, and depends on the fact that the amount of charge entering C_s during t equals the amount leaving it during T under steady state conditions. The charge Q_c is equal to the charge current, e_c/R_c, times the charge time t, and Q_d is equal to the discharge current e_d/R_d times the discharge

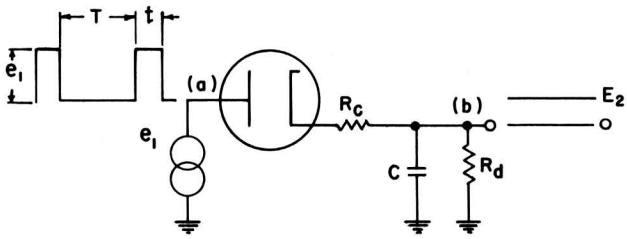
[2] *LB-494, Video Output Systems.*

time T. Equating the two charges results in the expression as shown for the ratio of e_c to e_d. The lower this ratio is, the more efficient the d-c restorer is at maintaining black-level. As can be seen, the controlling factors are the ratios of the charge to discharge path resistance and the discharge to charge time.

If it is assumed that all the charge path resistance is in the source and that the diode has zero forward resistance, the voltage at (b) cannot rise above 0. However, the voltage e_c, as called for by the equation, is still required to charge the capacitor and under these conditions it will be developed across the source resistance. The result is that the value of e_d in the output remains the same as that called for in the equation, but that e_c is clipped off and will not appear in the output. Since ordinary d-c restorers have both source and diode forward resistance, some clipping of the signal always takes place, and it becomes increasingly severe as the ratio of the required charge voltage e_c to the discharge voltage e_d increases.

Pulse Peak Detector

Fig. 3 shows a pulse peak detector. The time constant assumptions are the same as in the previous case. The input pulses are shown at point (a) and the rectified output at (b). In this case the voltage available for charging



$$Q_c = \frac{e_1 - E_2}{R_c} t \qquad Q_d = \frac{E_2}{R_d} T$$

BUT AT EQUILIBRIUM

$$Q_c = Q_d$$

$$\therefore E_2 = e_1 \frac{R_d}{R_d + \frac{T}{t} R_c}$$

Fig. 3 – Pulse peak detector.

C is equal to the difference in amplitude between the pulse height e_1 and the detected output E_2. The equations are set up in the same way as in the d-c restorer case by equating the charge and discharge of the capacitor C.

The resulting relationship is in the form of a resistance voltage divider equation. The principal feature of this equation is the fact that the charge resistance R_c enters the equation multiplied by the ratio of discharge to charge times, and consequently appears to be a much larger resistor than it actually is.

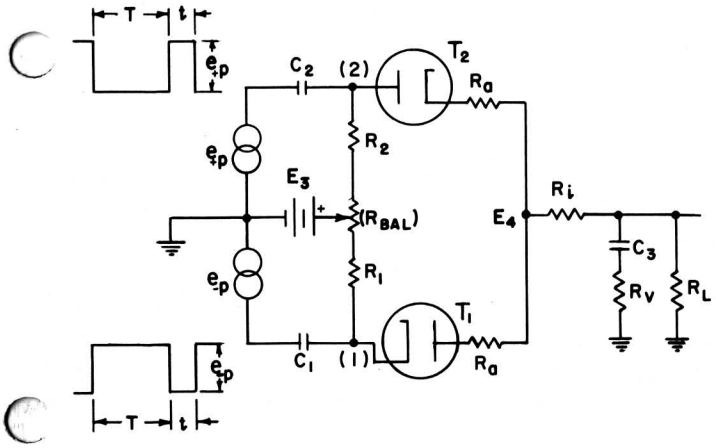
Analysis of Keyed Clamping Circuits

With the preceding examples as background, further consideration can now be given to the loaded keyed clamp. The circuit is shown in Fig. 4a redrawn for the purposes of analysis. Two equal amplitude push-pull pulses labeled e_{+p} and e_{-p} are supplied by the generators at the left of the figure. The two equal resistors both labeled R_a, are the sums of the diode forward resistance and pulse source impedance in the two branches of the circuit. Again it is assumed that the various RC time constants are long compared to the duration of the pulses which act on them, and in addition, that R_1 and R_2 are both much larger than R_a, and that the leakage resistance R_L, though not infinite, is still much larger than R_1 and R_2.

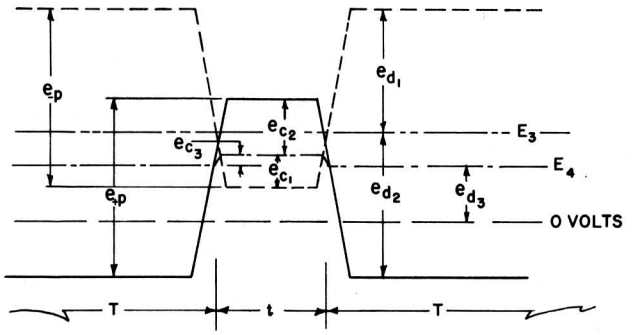
The circuit equations are set up in the same general way as in the two preceding cases. First we may note that when the circuit is in equilibrium the individual charge and discharge of each of the three capacitors C_1, C_2, and C_3 must be equal. In addition, the sum of the charges on these three capacitors is constant. Consequently the first group of equations is: $Q_{c1}=Q_{d1}$, $Q_{c2}=Q_{d2}$, $Q_{c3}=Q_{d3}$ and $Q_{c2}=Q_{c1}+Q_{c3}$

wherein the subscript c refers to the charge flowing during the pulse-on period t, and subscript d refers to the discharge flowing during the pulse-off period T. The numerical subscripts 1, 2, and 3 refer to the capacitors C_1, C_2 and C_3 respectively.

In order to obtain the required additional equations, the various voltage drops around the circuit due to the presence of the clampin



(a) Keyed clamping circuit.



(b) Details of clamping pulses.

Fig. 4 – Effects of leakage on clamping operation.

pulses e_{+p} and e_{-p} are added up. Fig. 4b is a somewhat exaggerated, expanded view of the pulses as they appear at the points labeled (1) and (2) of Fig. 4a, relative to the various d-c voltages involved in the circuit. In this figure E_3 was assumed to be some fixed positive potential above zero volts. The presence of the leakage resistance R_L causes the output voltage E_4 to be somewhat lower than it would be under open circuit conditions. Considering the positive going pulse which operates on T_2, it can be seen that T_2 will conduct when the pulse goes above the value of E_4. During this conduction time, the voltage E_4 rises due to the peak current flowing through R_V and R_i. This rise in voltage e_{c3} is the voltage available to charge C_3. The portion of the pulse voltage available for charging C_2 is then the difference between this peak voltage of E_4 and the peak voltage of the positive clamp pulse e_{+p} and is labeled e_{c2}. Similarly the voltage available for charging C_1 is difference between the peak voltages of E_4 and the negative clamp pulse e_{-p} and is labeled e_{c1}.

The discharge voltage of C_3, labeled e_{d3}, is substantially equal to the clamp output voltage E_4. Since during the discharge time T the diodes are nonconducting, C_1 and C_2 both discharge toward E_3, resulting in the discharge voltages e_{d1} and e_{d2} shown in the figure.

By adding up the voltages on the positive and negative pulses the following two equations are obtained:

$$e_{+p} = e_{d2} - (E_3 - E_4) + (e_{c2} + e_{c3})$$

and

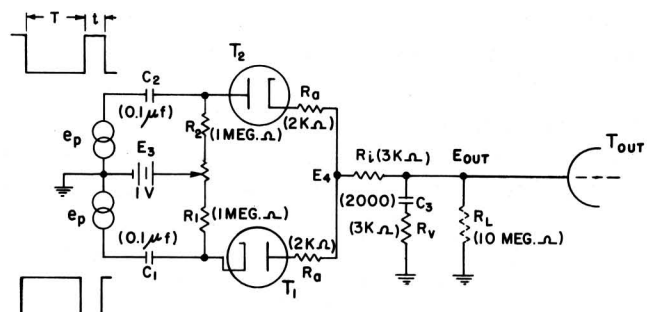
$$e_{-p} = e_{d1} + (E_3 - E_4) + (e_{c1} - e_{c3})$$

These relationships complete the group required for the development of the clamping circuit equation. Their solution is worked out in a conventional manner in the appendix to the present bulletin.

Design Considerations

The equation shown in Fig. 5 is the clamping circuit equation. τ is the ratio of pulse-off time to pulse-on time. R_a is the combined pulse source and diode forward resistance. R_s is the sum of the video source resistance R_v, and isolation resistance R_i. R_p is the parallel combination of $R_1 + R_a\tau$ and $R_2 + R_a\tau$. R_L is the leakage resistance.

The equation is useful in bringing out many of the factors involved in the design of



WHERE $\tau = T/t$, $R_s = R_i + R_v$, AND $R_p = \frac{(R_1 + R_a\tau)(R_2 + R_a\tau)}{(R_1 + R_a\tau) + (R_2 + R_a\tau)}$

Fig. 5 – Clamping circuit equation.

the circuit, especially insofar as stability of operation is concerned. For example, the values of the components shown in parentheses in Fig. 5 are more or less typical. If the ratio of pulse-off to pulse-on time (τ) is 40, and the bias voltage (E_s) is +1 volt, and the leakage resistance (R_L) is substantially infinite, the clamping level (E_{out}) is also +1 volt. However, if for some reason a leakage current of one-tenth microampere flows, the effective leakage resistance drops to approximately 10 megohms, and the calculated clamping level drops to approximately 0.93 volt. This voltage will probably not be stable since it is dependent on the value of the leakage resistance.

It can be seen from the equation that in order to minimize the drift effects of R_L, the right hand term in the denominator should be very small compared to unity. This requires that leakage resistance R_L be large, and the $R_p+R_s\tau$ term be small. Insofar as R_L is concerned, leakage in the coupling capacitor C_s, the diodes, and the tube sockets can cause trouble in isolated instances but these troubles can be avoided by employing reasonably high quality components in the circuit. However, a more serious problem exists in those instances when it is necessary to clamp the grid of a tube of a type which is prone to either gas currents or grid emission. Under these conditions the effective value of R_L may be sufficiently low to cause clamp level instability. In many cases it is possible to increase R_L by running the tube "cool", that is by operating the tube well within its rated dissipation and by reducing its filament voltage toward the lower limit of the manufacturer's tolerance.

Insofar as the $R_p+R_s\tau$ term is concerned, it is desirable to make it small. This requires that τ be as small as possible, that is, the clamp pulse be as long as the particular operating conditions permit. Moreover R_s, which is the sum of the video source resistance R_v and the isolation resistor R_i, and R_p, which is a combination of the resistors R_1, R_2 and $R_a\tau$, should be made very small compared to the leakage resistance R_L.

To be sure, these various resistances cannot be lowered without limit, for other factors are involved. For example, the factor which usually determines the lower limits of R_1 and R_2 is the amount of clamp pulse power available. This is because the clamp pulse source resistance in an actual circuit has some finite value and as R_1 and R_2 are lowered, C_1 and C_2 discharge more heavily so that the peak charge current supplied to the diodes must also increase. Consequently the pulse source is more heavily loaded and the pulse voltage drops. It may be noted that since the diode forward resistance follows a three-halves power law, it decreases with increasing peak current. Consequently, R_a is lowered as the resistances of R_1 and R_2 are reduced, a factor which is beneficial insofar as clamp circuit stability is concerned.

The lower limit of clamp pulse voltage required depends on the largest amplitude video signal to be clamped. In order to prevent video signals from causing the diodes to conduct, the back bias voltages must be at least as large as the largest video signals, consequently the clamp pulses themselves must be at least this large and perhaps be 25 to 50 per cent larger. Keeping the clamp pulse height within these limits is desirable since it minimizes the amount of spurious clamp signal which can appear in the video signal so that a small isolation resistor, R_i, is sufficient. In addition, as can be seen from the fraction in the numerator of the clamping circuit equation, increasing the pulse height makes the clamp output level more sensitive to a possible drift in the resistance values of R_1 and R_2. As a final observation it may be noted that the fraction in the numerator of the equation also indicates that one difficulty associated with setting the clamp level by varying the relative sizes of R_1 and R_2 is that the clamp level becomes sensitive to variations in clamp pulse amplitude.

Roland N. Rhodes

Appendix

Development of the clamping circuit equation. (see Fig. 4)

$$Q_{c3} = Q_{d3} \tag{1}$$

$$\therefore \frac{e_{c3}}{R_v+R_i}\, t = \frac{e_{d3}}{R_L}\, T \tag{1a}$$

$$e_{d3} = E_4 \tag{1b}$$

$$\therefore e_{c3} = \frac{R_s\tau}{R_L} E_4 \tag{1c}$$

where $T/t = \tau$ and $R_v+R_i = R_s$

$$Q_{c2} = Q_{c1} + Q_{c3} \tag{2}$$

$$\therefore \frac{e_{c2}}{R_a}\, t = \frac{e_{c1}}{R_a}\, t + \frac{e_{c3}}{R_s}\, t \tag{2a}$$

$$\text{or } e_{c3} = \frac{R_s}{R_a\tau}\,(e_{c2}-e_{c1}) \tag{2b}$$

and substituting from Eq. (1c)

$$E_4 = \frac{R_L}{R_a\tau}\,(e_{c2}-e_{c1}) \tag{2c}$$

$$Q_{c1} = Q_{d1} \tag{3}$$

$$\therefore \frac{e_{c1}}{R_a}\, t = \frac{e_{d1}}{R_1}\, T \tag{3a}$$

$$\text{or } e_{d1} = \frac{R_1}{R_a\tau}\, e_{c1} \tag{3b}$$

from Fig. 4

$$e_{d1} = e_p - (e_{c1}-e_{c3}) - (E_3-E_4) \tag{4}$$

and combining Eqs. (4), (3b) and (1c)

$$e_{c1}\left(\frac{R_1}{R_a\tau}+1\right) = e_p - E_3 + E_4\left(\frac{R_s\tau}{R_L}+1\right) \tag{4a}$$

$$\therefore e_{c1} = \frac{R_a\tau}{R_L}\,\frac{R_1(e_p-E_3)+E_4(R_s\tau+R_L)}{R_1+R_a\tau} \tag{4b}$$

$$Q_{c2} = Q_{d2} \tag{5}$$

$$\therefore \frac{e_{c2}}{R_a} t = \frac{e_{d2}}{R_2} T \qquad (5a)$$

$$\text{or} \quad e_{d2} = \frac{R_2}{R_a \tau} e_{c2} \qquad (5b)$$

from Fig. 4

$$e_{d2} = e_p - (e_{c2}+e_{c3})+(E_3-E_4) \qquad (6)$$

and combining Eqs. (6), (5b) and (1c)

$$e_{c2} \left(\frac{R_2}{R_a \tau}+1\right) = e_p+E_3-E_4\left(\frac{R_s \tau}{R_L}+1\right) \qquad (6a)$$

$$\therefore e_{c2} = \frac{R_a \tau}{R_L} \cdot \frac{R_L(e_p+E_3)-E_4(R_s \tau+R_L)}{R_2+R_a \tau} \qquad (6b)$$

Combining Eqs. (6b), (4b), and (2c);

$$E_4 = R_L \left[\frac{e_p+E_3}{R_2+R_a \tau} \cdot - \frac{e_p-E_3}{R_1+R_a \tau}\right] - E_4 \ (R_s \tau+R_L)\left[\frac{1}{R_2+R_a \tau} + \frac{1}{R_1+R_a \tau}\right] \qquad (7)$$

$$\therefore E_4 = \frac{E_3+e_p \ \frac{R_1-R_2}{R_1+R_2+2R_a \tau}}{1+\frac{R_s \tau}{R_L}+\frac{1}{R_L}\left[\frac{(R_2+R_a \tau)(R_1+R_a \tau)}{R_1+R_2+2R_a \tau}\right]} \qquad (7a)$$

but $[(R_2+R_a\tau)(R_1+R_a\tau)/R_1+R_2+2R_a\tau]$ is the parallel resistance of $(R_1+R_a\tau)$ and $(R_2+R_a\tau)$ which hereafter is called R_p; and E_4 is substantially equal to the output clamping level E_{out}.

$$\therefore \boxed{E_{out} = \frac{E_3+e_p \ \frac{R_1-R_2}{R_1+R_2+2R_a \tau}}{1+\frac{R_p+R_s \tau}{R_L}}} \qquad (8)$$