Silicon Double-Diffused Mesa Series (for amplifiers)

TRANSISTOR TECHNICAL NOTES

HUGHES SEMICONDUCTOR DIVISION

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DOUBLE-DIFFUSED MESA TRANSISTORS FOR HIGH FREQUENCY APPLICATIONS

Silicon transistor technology has taken a dramatic step forward with the development of the double-diffused mesa transistor. Types 2N1196 and 2N1197, covered by this report, make practical for the first time the design of all-transistor amplifiers operating at frequencies up to 100 mc.

The result is to upgrade the potential reliability of communication, telemetering and similar electronic equipments which up till now have not been adaptable to solid-state design. The opportunity is now present for a radical reduction in equipment size and weight and an equally important improvement in the capability of the equipment to withstand severe environments.

The high frequency characteristics of the new Hughes transistors are literally "built in" to the semiconductor elements. The diffusion process (next page) differs distinctly from any manufacturing process ever used before in the semiconductor industry. The "doping" of semiconductor metals has generally taken place in the liquid phase on a batch basis. This has necessarily involved a wide variance in physical and electrical characteristics from lot to lot. The diffusion process, by contrast, is effected by exposing a *solid* semiconductor metal to a *gaseous* impurity. The diffusion of the impurity into the metal surface is dictated by physical laws that are unchanging. The result is a level of uniformity that has never been achieved before.

The precision allowed by the diffusion process has permitted Hughes to tailor transistors specifically to the job of high frequency amplification. The boundries between PNP layers can be controlled to millionths of an inch. Capacitance across the transistor (see Figure 1H) is sharply reduced and the base width held within very strict limits. Both factors affect the high frequency characteristics of a transistor. By exercising close manufacturing controls over every step in the process, Hughes has developed a high-frequency unit that opens up entirely new areas of application for semiconductor devices.

THE DOUBLE DIFFUSION PROCESS

The silicon ingot from which the "diffused" transistor dice are derived is a single crystal ingot approximately one inch in diameter (Figure 1A). Thin wafers are sliced from the ingot, lapped, and polished to a mirror finish. This "finished" surface of the silicon is very exacting and requires a technique comparable to the optical polishing of the most precision lenses.

The silicon slice is "doped" by exposure to arsenic vapor at high temperatures in special furnaces. The arsenic diffuses from the surface of the silicon slice inward to a definite depth, creating what will be the "N" portion of the finished transistor silicon.

SPECIFICATIONS

Absolute Maximum Ratings (25°C)	*2N1196*	*2N1197*
Collector to emitter voltage (V_{CEO}) (I_{CEO}=−100 μA)	−40 volts	−40 volts
Power Gain (P_G) (I_E=2mA, V_{CE}=10V)	24 dB min	20 dB min
Output Capacity (C_{ob}) (V_{CB}=−10V, I_E=0, f=140 Kc)	4 μμf max	4 μμf max
Emitter to base voltage (V_{EBO}) (I_{EBO}=−100 μA)	−3 volts	−3 volts
Power dissipation	250 mw	250 mw
Power derating	1.8 mw/°C	1.8 mw/°C
Storage temperature range	−65°C to +160°C	−65°C to +160°C
Operating temperature range	−65°C to +200°C	−65°C to +200°C

A photo sensitive resin is then employed to mask the silicon slice with parallel stripes of protected and exposed metal (Figure 1E). After the masking is completed, the silicon slice is again exposed to an atmosphere of vaporized metal at elevated temperatures. This time, boron is used.

The diffusion of boron into the surface of the silicon inward "dopes" the metal, creating a "P" type emitter region. The result is an array of stripes, Figure 1F, inside the surface of the silicon, each alternately "doped" N and P. These, together with the parent silicon slice will constitute the PNP transistor structure.

Small square areas are then described on the silicon surface, again employing a photo-sensitive resin process. After etching, these small, protected squares become tiny plateaus—or mesas. Since an N-P boundary bisects the mesa surface, each is a complete transistor structure in itself. The diffused regions of N and P type silicon represent the base and emitter of the transistor, while the body of the silicon slice, which came from a P-type ingot, serves as the collector terminal.

The thin silicon slice with its hundreds of tiny PNP mesas is cut into small squares or dice. Each die is mounted on a gold-clad nickel tab, Figure 2A, which serves both as the transistor support and the collector terminal. This same tab also acts as a heat dissipating media.

The emitter and base contacts are made directly to the silicon surface by a unique thermo-compression bonding process. The transistor sub-assembly, with leads attached, is now ready for incorporation into the final package. The unit is mounted on the support "header" assembly and hermetically sealed within an ambient atmosphere conducive to long life and reliability. The fabrication process provides for extreme rugged utilization, sustaining the requirements set forth by MIL-T-19500A.

PUTTING THE DOUBLE DIFFUSED MESA TRANSISTOR TO WORK

The principle application for double diffused mesa transistors with characteristics such as those demonstrated by Types 2N1196 and 2N1197 will be in amplifiers, oscillators and similar circuit elements operating at medium to high frequencies (up to 100 mc).

This is a new area of application for semiconductor devices, requiring new design criteria. The relationship of gain to frequency, for example, is one of the most important characteristics to be determined in evaluating the usefulness of a particular transistor type in an amplifier circuit which has to meet particular operating specifications.

FIG. 1 Diffusion

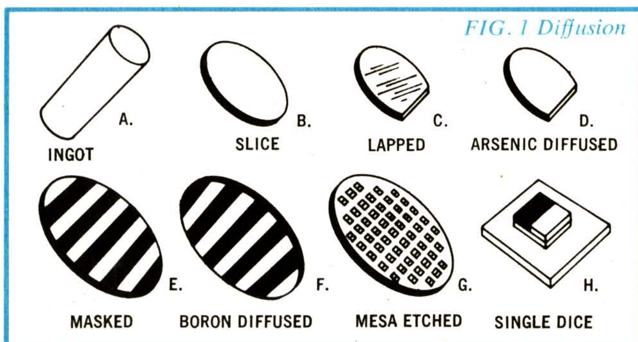


FIG. 2A Mount Dice

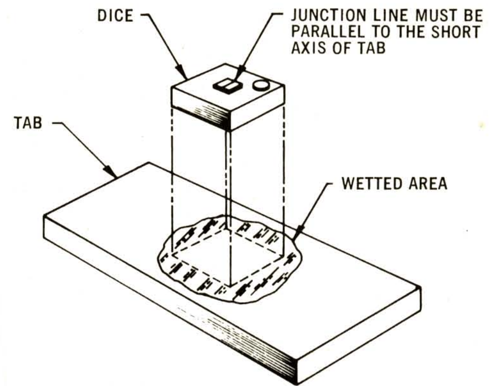


FIG. 2B Bond Leads

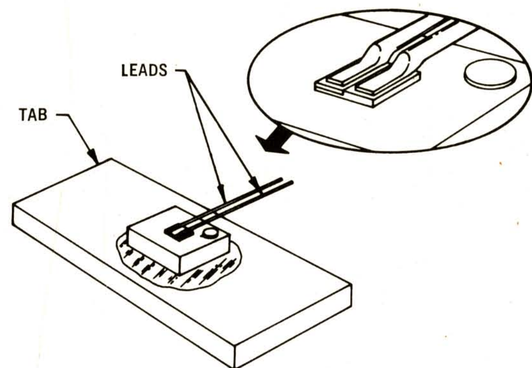


FIG. 2C Weld Tab to Header Posts

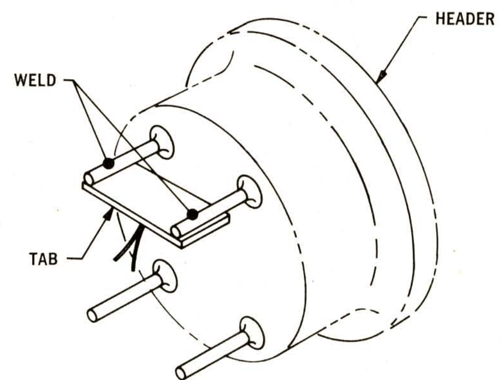


FIG. 2D Weld Leads to Header Posts

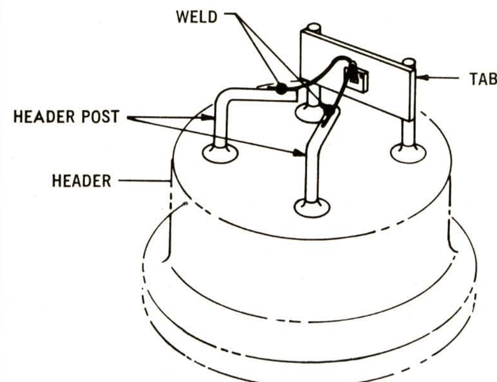
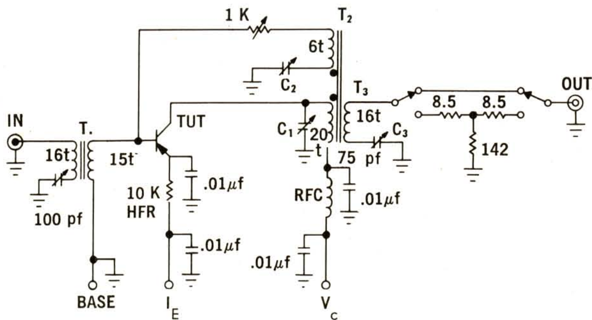


FIG. 3. Power Gain Measurement Circuit



1. XFMRS wound on General Ceramics Corp. Q-Z torodial cores
2. C_1, C_2, C_3 100pf cut to size
3. Vium is Boonton Electronics Corp. RT Voltmeter, type 91-CA
4. Amplifier is Lel Inc., Model IF-31—impedance of 50 ohms
5. Switching—Danburg Knudsen, Type CR56

FIG. 4. Block Diagram for Power Gain

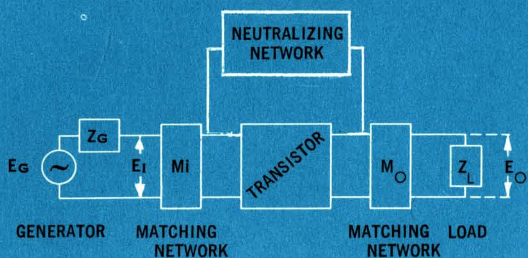


FIG. 5. High Frequency Parameter Variation with Emitter Current ($V_C = -6V$)

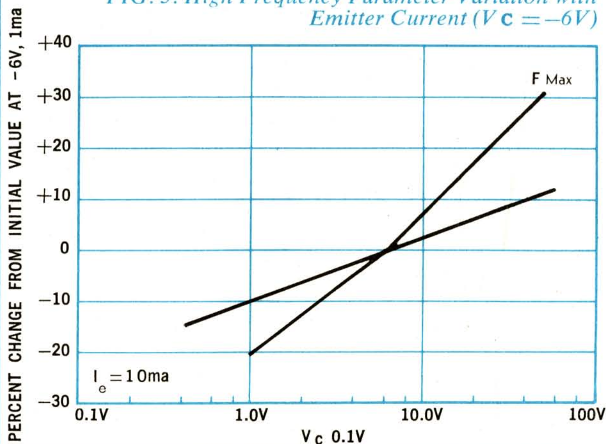
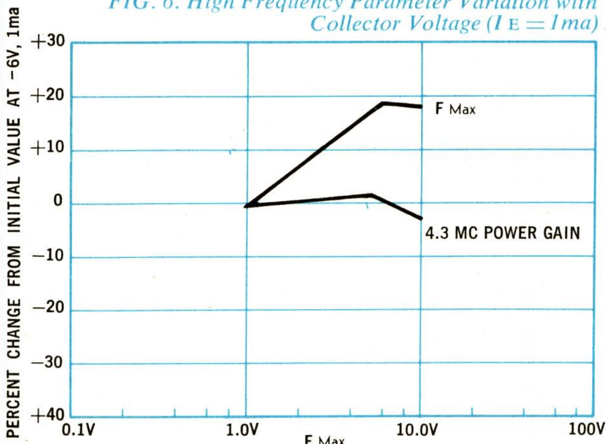


FIG. 6. High Frequency Parameter Variation with Collector Voltage ($I_E = 1ma$)



"Unilateral power gain" and "maximum frequency of oscillation" are two characteristics of particular interest to the engineer designing transistorized IF strips, amplifiers and oscillators. The sections below describe how these values are determined and used.

UNILATERAL POWER GAIN

The unilateral power gain of a transistor is the ratio of available power at the output terminals of a single stage amplifier incorporating the transistor, to the power delivered to the input with a lossless feedback network connected so as to make the reverse power gain zero.

To get the transistor unilateralized or as close to that condition as possible, the power gain is measured in a tuned input, tuned output, neutralized circuit employing capacitance tuning and matching.

The circuit used to make this measurement is shown in Figure 3. The input and output circuits are built to match a 50 ohm source and load respectively. Measuring the open circuit generator voltage and, knowing R_G, the available power of the generator can be calculated.

If a lossless, conjugate matching network is then placed between the generator and the transistor input, the available generator power will be delivered to the transistor itinput. Similarly, by knowing R_L and the voltage across it, E_O, the power delivered to the load can be calculated. With a lossless, conjugate matching network between transistor output and load, the available output power of the transistor is delivered to the load.

A block diagram, Figure 4, of the circuit is shown which illustrates the switching performed in the measurement. Two relays are used to reverse the test jig for neutralization and two relays are used to switch the voltmeter from the output to the input for the actual measurement of power gain.

MAXIMUM FREQUENCY OF OSCILLATION

The maximum frequency of oscillation, f max, is that frequency where the unilateral power gain of the transistor drops to unity or "O" db gain.

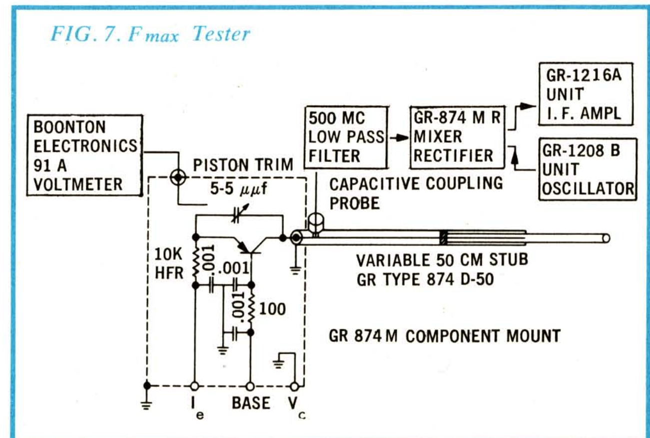
The maximum frequency of oscillation, f max, and the power gain, U, can be related to the equivalent circuit parameters of the transistor by the following equations:

$$U = \frac{\alpha f\alpha b}{8\pi r_b' C_c f^2}$$

$$f\,max = \sqrt{\frac{\alpha f\alpha b}{8\pi r_b' C_c}}$$

$$U\,max = \left(\frac{f\,max}{f}\right)^2 \quad \text{or} \quad PG = 20\ \text{Log}\ \frac{f\,max}{f}\ \text{dB}$$

FIG. 7. Fmax Tester



These equations in effect provide an approximate gain-versus-frequency relationship. Once f max has been determined, the power gain at lower and more interesting frequencies may be roughly calculated.

The measurement of f max may be accomplished by employing the circuit illustrated in Figure 7. The circuit is constructed around a General Radio type 874 M component mount with a variable stub plugged directly into the connector provided. A capacitive coupling probe, used in conjunction with the Boonton 91A RF voltmeter as an oscillation indicator, is mounted on the cap of the component mount. A modified General Radio tee connector is placed between the jig and the transmission line for the purpose of coupling to a frequency indicator. The coupling is capacitive.

In operation, the tuning line is shortened gradually while simultaneously adjusting the feedback for highest output as indicated by the voltmeter. At the point where oscillation just stops, the frequency is measured by the receiver. It is expected that this circuit will operate up to about 400 mc.

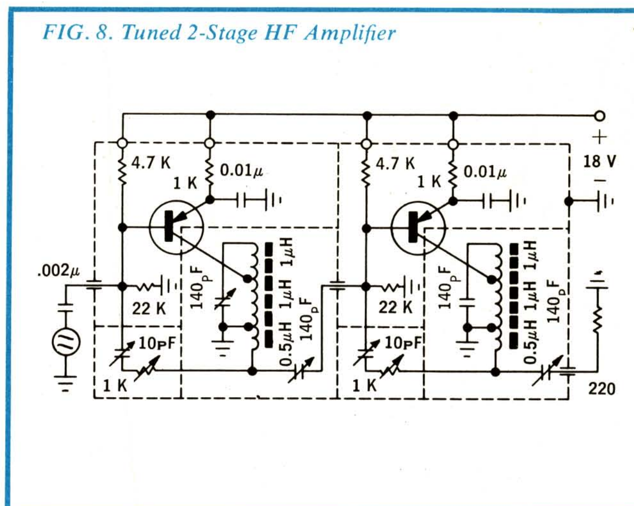
TYPICAL CIRCUIT—TUNED TWO-STAGE HIGH FREQUENCY AMPLIFIER

The application of double-diffused mesa transistors in a typical amplifier design is illustrated in Figure 8. The amplifier is a two-stage unit employing two High-Q tuned circuits. Inductance is provided by coils wound on ferrite tubing. The arrangement of the coils on the tubing is shown in Figures 9 and 10.

Figure 11 shows the gain-versus-frequency characteristics of the amplifier using the coil arrangement represented by Figures 9 and 10. In the case of Figure 10, the curve shows a maximum power gain of 44 db, bandwidth 200 kc, stagger tuned to 12 and 13 Mc, a power gain of 30 db, and bandwidth of 1.6 Mc.

Figure 12 shows the result of adding a third tuned circuit at the input. With synchronous tuning the maximum power gain is approximately 40 db and the bandwidth 700 kc. Stagger tuning to 12.5 Mc, 11 Mc, and 14 Mc results in a 3 Mc bandwidth.

FIG. 8. Tuned 2-Stage HF Amplifier



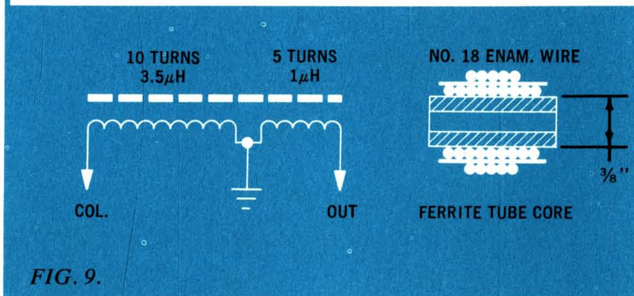


FIG. 9.

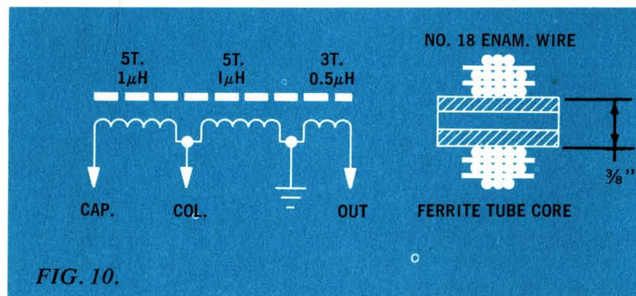


FIG. 10.

FIG. 11. 2-Stage Amplifier—2 High-Q Tuned Circuits

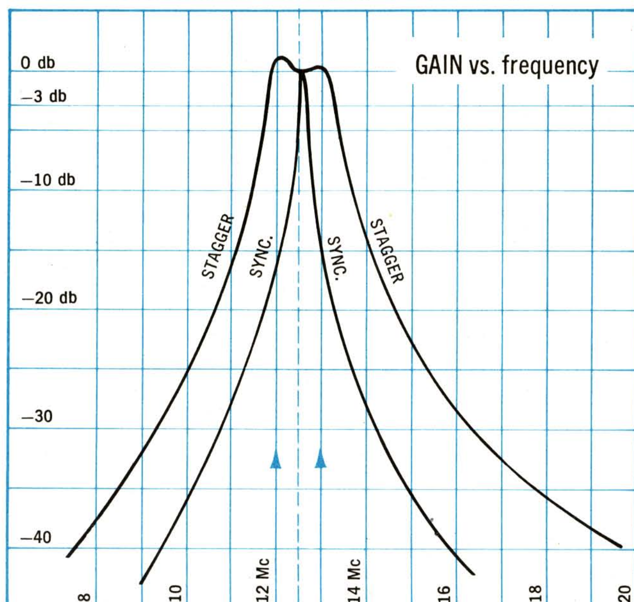
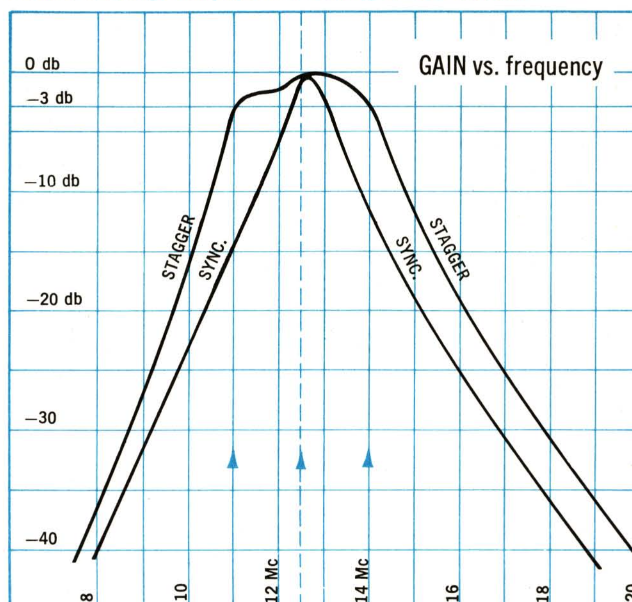


FIG. 12. 2-Stage Amplifier—3 Low-Q Tuned Circuits



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