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(Application Lab Report 701A)

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APPLICATION LAB REPORT 701A

Transistor Guide For Communications Circuit Designers

By C. R. Gray and T. C. Lawson

Introduction

The purpose of this report is to provide in one publication a summary of the basic ground rules which should be followed in designing transistorized communications circuits. The report assumes a working knowledge of the terms and circuits used by communications designers. It does not delve into the design of interstage coupling networks, etc. Rather it points out the areas which the designer should consider when building transistorized circuits. A number of rules of thumb are included in an attempt to provide a designer with a practical understanding of the results which can be expected with transistorized communications equipment.

Important Transistor Parameters in Communications Circuits

In the design of communications circuits there are a number of parameters which must be understood before a design is attempted. Considerable confusion has existed over the validity and the relative merits of the various parameters which specify and categorize the characteristics of the communications transistor. At least three terms are commonly referred to in describing the frequency capabilities of present day transistors. It is important that each of these be understood and properly applied to each application. These parameters are f_{max}, f_T and f_{α_b}.

f_{max} is defined as the theoretical maximum frequency at which the transistor could oscillate. It is, of course, also equal to the frequency at which the power gain is unity. Figure 1 shows a sketch of the variation of unilateralized power gain versus frequency for most present day transistors. All transistors of the electrochemical family including MADT's, SADT's, SBT's, MAT's and SPAT's follow curves of this general shape with a slope beyond the rolloff region of 6 db per octave. Thus every time the frequency is doubled, the gain falls 6 db. The intersection of the rolloff with the horizontal axis which represents 0 db power gain or an absolute power gain of one, is then f_{max}. Therefore, in a tuned amplifier which is unilateralized, if either f_{max} is known or the unilateralized power gain at some frequency on this slope is known, it is very easy to calculate the expected power gain over the entire slope. The power gain in the flat region of the curve is dependent upon the low frequency current gain of the transistor. In the sketch of Figure 1, the maximum available gain (MAG) is shown as about 55 db. This will vary somewhat depending upon the current gain of the device and input and output impedances. However, as will be discussed later, present day transistors are unstable throughout most of this flat region unless they are perfectly unilateralized. The unilateralization networks are extremely complex at these low frequencies and it is difficult to find a simple network of fixed components which will provide adequate unilateralization for a large number of transistors. It is, therefore, common practice to obtain stability in this low frequency region by mismatch. The maximum useable gain under mismatch conditions is usually in the neighborhood of 40 db. Therefore, for practical considerations it is usually wise to not extend the power gain scale above 40 db. Thus with f_{max} known and the 40 db line assumed, it is very easy to completely reconstruct the power gain versus frequency curve of a transistor. It should also be noted that a 6 db per octave slope is equal to 20 db per decade. If 40 db is assumed, as the maximum useful gain, the knee of the curve as shown in Figure 1 occurs at $\frac{f_{max}}{100}$ (2 decades).

f_{max}, therefore, is the most useful parameter in defining the power gain of tuned unilateralized amplifiers. In specifying transistors for tuned applications either the f_{max} or the power gain at some frequency on the slope should be specified. If the frequency of operation is in the flat region, then the low frequency current gain of the device should be specified. While the low frequency power gain is different for the three different connections of the transistor (common emitter, common base, and common collector) the unilateralized power gain is the same throughout the 6 db region and, therefore, all three connections have the same f_{max}.

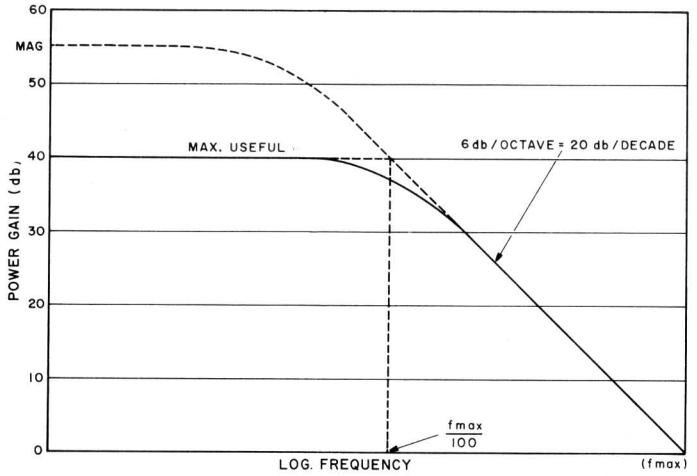


FIGURE 1 UNILATERALIZED POWER GAIN VS FREQUENCY

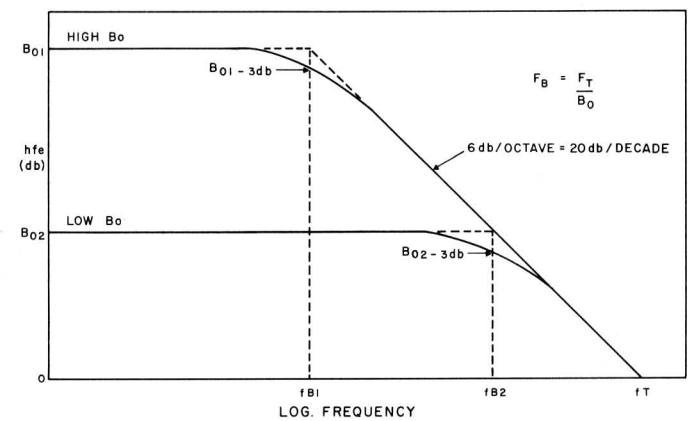


FIGURE 2 COMMON EMITTER CURRENT GAIN (h_{fe}) VS FREQUENCY—OUTPUT SHORT CIRCUITED

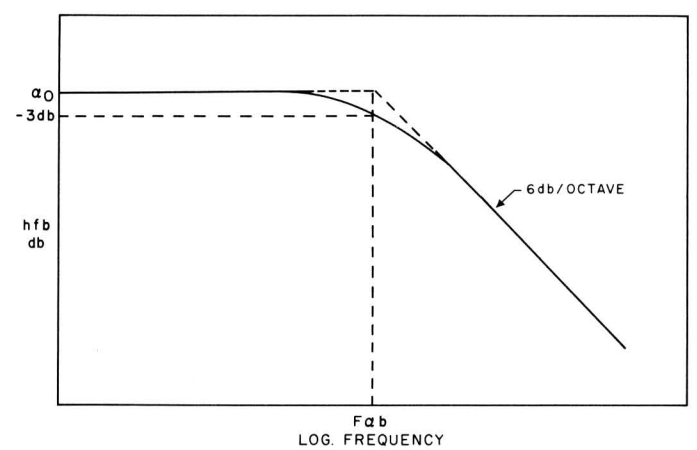


FIGURE 3 COMMON BASE CURRENT GAIN (h_{fb}) VS FREQUENCY—OUTPUT SHORT CIRCUITED

f_T is the gain bandwidth product of the transistor. It is defined as the frequency at which the common emitter forward current gain (h_{fe}) is equal to unity when the output is short circuited. Figure 2 shows a plot of h_{fe} as a function of frequency. Again the rolloff is 6 db per octave. The low frequency current gain is often referred to as β_o. A term sometimes associated with f_T is the beta cutoff frequency, f_β. This is the frequency at which h_{fe} is down 3 db and, of course, also defines the knee of the curve shown in Figure 2. It can be shown that

$$f_\beta = \frac{f_T}{\beta_o}.$$

Figure 2 also shows that the transistors having the same f_T but different β_o's have considerably different f_β's. This effect will be discussed in more detail under Video Amplifiers.

The use of f_T should, in general, be limited to video amplifier and switching circuits. While it is true that f_T defines the common emitter current gain at all frequencies, once β_o is known, it does not guarantee power gain unless precise specifications of input and output impedance are given.

The alpha cutoff frequency ($f_{\alpha b}$) is defined as the frequency at which the common base forward current gain is down 3 db from its low frequency value. Again the output is short circuited. Figure 3 shows a sketch of the common base current gain (h_{fb}) as a function of frequency. The low frequency current gain is often referred to as α_o.

The use of the term $f_{\alpha b}$ is rapidly being abandoned in the communications field for several reasons. Like the term f_T, $f_{\alpha b}$ only indicates current gain and can not be used as a measure of the power gain unless the input and output impedances are accurately known. Secondly, it is a common base parameter and most communications type circuits are common emitter. Thirdly, with the advent of the diffused base transistors, the alpha cutoff frequency is not a good measure of the frequency capabilities of the transistor. About the only time $f_{\alpha b}$ is useful in present day transistors is when the transistor is used as a grounded base video amplifier in extremely wide band video applications.

There are a number of relationships which are useful in converting from one of these parameters to the other, as follows:

$$f_{max} = \sqrt{\frac{\alpha_o f_T}{8\pi r_b' C_c}} \approx \sqrt{\frac{f_T}{8\pi r_b' C_c}} \qquad (1)$$

This equation indicates a relationship between the two most useful high frequency parameters. It also indicates that it is possible to improve one or the other of these parameters by changing $r_b'C_c$, providing the other conditions remain constant. As noted earlier, f_{max} defines high frequency tuned amplifier performance and f_T switching and video amplifier performance. It is, therefore, possible to optimize transistors for either f_{max} or f_T depending on the application. The electrochemical family of precision etch transistors are opti-

mized for these parameters depending upon the application. The ability to control accurately the various physical characteristics of the transistor makes this process ideally suited to manufacture transistors which have been specifically designed for each particular application.

In most diffused base transistors, f_T is approximately half $f_{\alpha b}$. In most homogeneous base transistors, f_T is approximately 85% of $f_{\alpha b}$.

Circuit Configurations

Three basic circuit configurations exist for use in transistor circuits. They are the common emitter, common base and common collector (emitter follower).

Common Emitter

This connection is the most widely used in communications circuits. It provides the highest current gain (h_{fe}) and is, therefore, nearly always used at frequencies which are in the flat portion of the power gain versus frequency characteristics.

In high frequency applications, as was noted earlier, the f_{max} and power gain are the same for all unilateralized configurations. Therefore, it is possible to obtain the same high frequency tuned amplifier power gain with all three connections. However, the common emitter amplifier has two distinct advantages in high frequency tuned circuits. The first of these is that the feedback at these frequencies between collector and base is degenerative. Thus the transistor is inherently stable in the high frequency common emitter connection. Neutralization provides a slight increase in gain at these frequencies, usually 1 to 3 db. The second factor is that it has been shown both mathematically and experimentally that a common emitter neutralized amplifier provides more stable operation, that is, less variation in gain and bandwidth from transistor to transistor than a similar common base amplifier. It is, therefore, recommended that common emitter neutralized amplifiers be used wherever possible for tuned communications applications at frequencies on the 6 db per octave slope. At frequencies above 300 mc where neutralization is difficult and gain very important, it may be desirable to use the common base connection.

Common Base

The unneutralized common base configuration provides slightly more gain at high frequencies than the neutralized common emitter. This is because the collector to emitter feedback in this connection is regenerative. The increase in gain is usually about 1 to 3 db depending upon the feedback capacity of the transistor. However, because of the inherent instability of this connection, its use is not recommended except at UHF frequencies where gain is extremely important. Experience has shown considerably more production difficulties with the common base connection.

Common Collector

The common collector configuration is used usually as an impedance matching device. The input impedance is given approximately by

$$Z_{in} \approx h_{fe} R_L. \tag{2}$$

The output impedance is given approximately by

$$Z_{out} \approx \frac{R_g}{h_{fe}} \tag{3}$$

where h_{fe} in both cases is the current gain at the particular frequency in question. Thus, this connection may be used to provide a high input impedance in applications such as an amplifier following a detector or when driving from a high impedance source. It provides convenient matching into the base of the following amplifier.

Low Frequency Gain

The low frequency gain of the three connections is dependent to a large extent on the ratio of the load resistance to the output resistance of the transistor. The common emitter configuration always has the highest gain for a given ratio of these two resistances. The common collector power gain approaches the common emitter power gain at very small ratios of load to output resistance. The common base power gain approaches the common emitter power gain at very large ratios of load to output resistance. Therefore, there is a value of load to output resistance at which the common base and common collector gains are equal and cross. This occurs at gains of about 15 to 20 db.

Noise Figure

Figure 4 shows a sketch of the variation of noise figure with frequency. For most germanium transistors the flat portion of the curve occurs at a noise figure of between 3 and 4 db. The low frequency noise figure rises with decreasing frequency and approaches a slope of 3 db per octave. The high frequency noise figure rises with increasing frequency and approaches a slope of 6 db per octave. A slight modification of Nielson's[1] equation (4) shows the variation of noise figure with transistor parameters.

$$F = 1 + \frac{r_b + \frac{r_e}{2}}{R_g} + \frac{(r_b + r_e + R_g)^2}{2\beta_o r_e R_g}\left[1 + \left(\frac{f}{\sqrt{1-\alpha_o} f_T}\right)^2\right] \tag{4}$$

This equation is composed of three sections. A constant, a term representing the resistive contribution of the input circuit and a term representing the shot noise of the transistor. When $f_T >> f$ the frequency dependent term drops out and the theoretical noise figure is a function of the source resistance (R_g), the intrinsic resistive elements of the transistor and β_o. If one assumes a matched condition and also assumes that the noise contribution of the source resistance and the intrinsic transistor resistance are identical in nature, then the noise contribution of the source and the transistor will be equal and the noise figure will be 3 db.

1. Behavior of Noise Figure in Junction Transistors—E. G. Nielson *Proc of IRE*, July 1957—Pages 957-963.

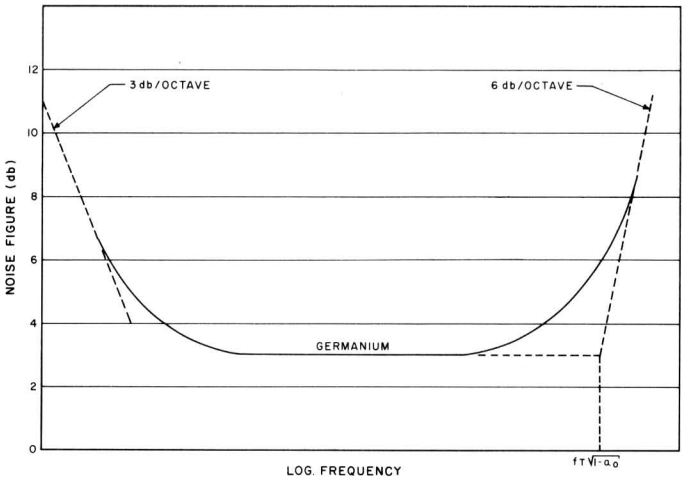


FIGURE 4 TRANSISTOR NOISE FIGURE VS FREQUENCY

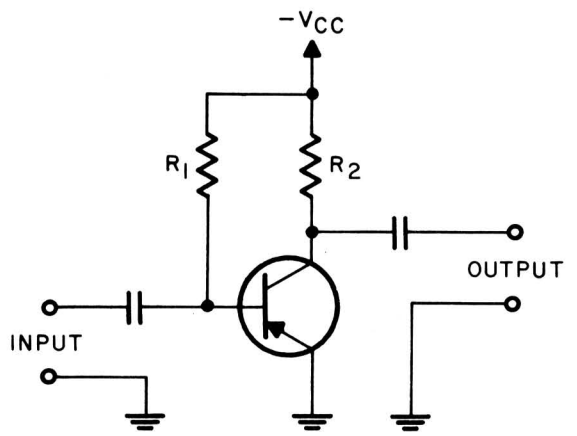


FIGURE 5 SIMPLE COMMON-EMITTER BIAS CIRCUIT

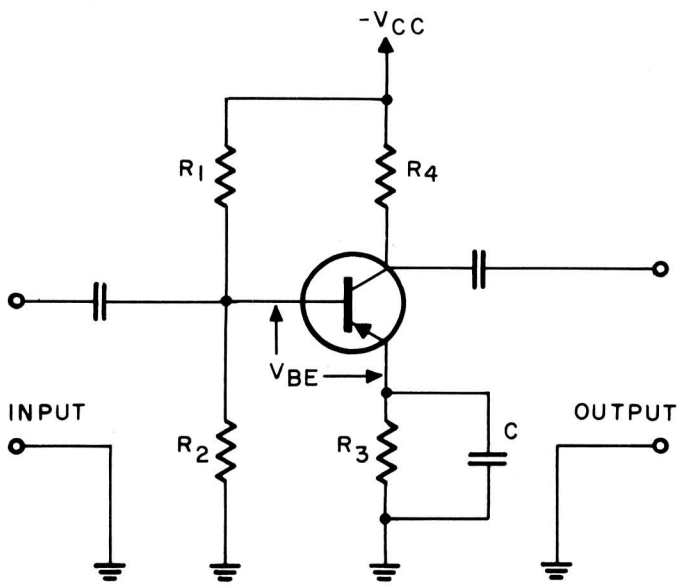


FIGURE 6 SIMPLE COMMON-EMITTER BIAS CIRCUIT WITH STABILIZATION

By mismatching the input some improvements may usually be obtained in the noise figure. However, from a practical standpoint it is usually well to consider the noise figure through the flat portion of the curve at about 3 to 4 db.

The low frequency noise figure knee is difficult to define, however, as a general rule, the higher the frequency of the transistor, the higher the frequency of this knee. To make a good low noise high frequency transistor the high frequency knee must be moved up in frequency. In general, when this is done the low frequency knee also moves up in frequency at the same time but not necessarily by the same amount. In present VHF and UHF transistors of the MADT family the low frequency knee occurs in the range of 10 to 100 kc depending upon the f_{max} of the transistor.

While theory indicates that the high frequency knee occurs at about $f_T \sqrt{1 - \alpha_o}$, measurements have shown that this knee is fairly broad and that the high frequency noise figure slope does not approach the 6 db per octave region until the frequency is considerably greater than the knee. As a general rule of thumb it appears that the high frequency noise figure of most transistors hits the 6 db per octave slope at about $\frac{f_{max}}{2}$. At about $\frac{f_{max}}{20}$ most transistors are down to the flat portion of the curve (3 to 4 db).

The noise figure of high frequency silicon transistors is generally 3 db higher than that of germanium types with similar high frequency characteristics. However, the noise figure of low and medium frequency silicon types is about the same as that of low and medium frequency germanium types.

For the electrochemical family of transistors the optimum high frequency noise figure occurs at about the same operating point as the optimum gain. This is usually about 1 to 3 ma collector current. At lower frequencies the optimum noise figure usually occurs at a current less than the current for optimum gain, normally 1 ma or less.

Biasing and DC Stability

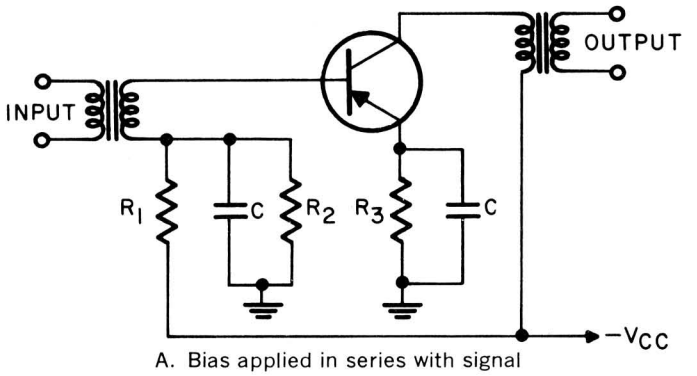
In most communications circuits, the transistor is operated at a DC operating point which must be established by applying DC voltages or currents to the unit. The selection of the DC operating point will depend upon the particular application; but once this point is selected, a bias circuit must be designed which will hold the transistor at this operating point.

A simple bias circuit for a common-emitter amplifier is shown in Figure 5. The DC base current in this type of circuit is approximately given by

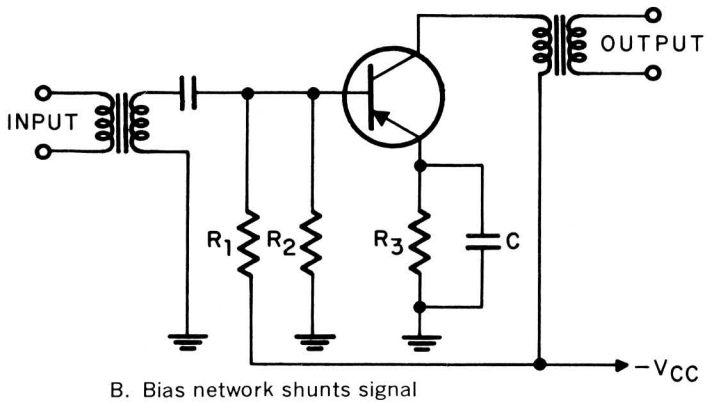
$$I_B = \frac{V_{CC}}{R_1} . \qquad (5)$$

Since $I_C = h_{FE} I_B$, then

$$I_C = h_{FE} \frac{V_{CC}}{R_1} \qquad (6)$$

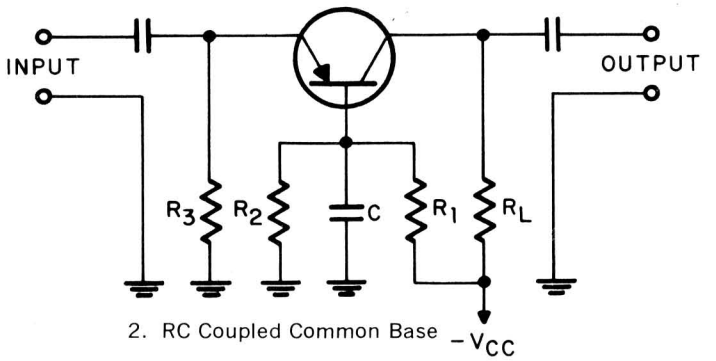


A. Bias applied in series with signal

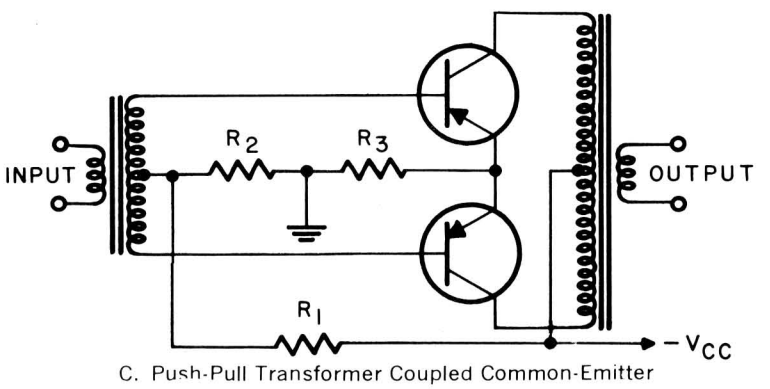


B. Bias network shunts signal

1. Transformer Coupled Common-Emitter



2. RC Coupled Common Base



C. Push-Pull Transformer Coupled Common-Emitter

FIGURE 7· TYPICAL COMMUNICATIONS BIAS CIRCUITS

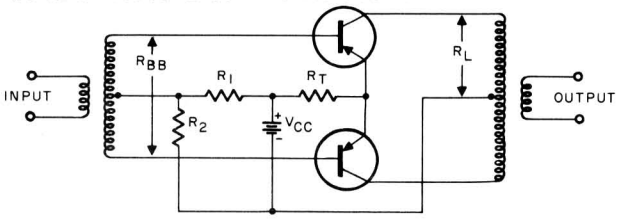


FIGURE 8 CLASS B PUSH-PULL AMPLIFIER

This means that for a particular transistor type, the shift of DC collector current in a fixed circuit is a function of the beta spread. If the operating point is critical for the intended application, this type of biasing will not suffice.

Figure 6 is a common-emitter bias circuit with DC stability. A stability factor may be defined as the ratio of the resistance in the base circuit to the resistance in the emitter circuit. A good value for this ratio is 3, however, a lower ratio would give better stability. A stability factor above five is not recommended for most communications circuits.

The emitter current (approximately the same as the collector current) for a bias arrangement similar to the circuit of Figure 6 may be calculated from

$$I_E = \frac{V_{CC}\left(\frac{R_2}{R_1 + R_2}\right) - V_{BE}}{R_3 + \frac{R_1 R_2}{h_{FE}(R_1 + R_2)}} \qquad (7)$$

$V_{BE} \approx 0.2$ v for germanium types

A close estimate of the collector current may be quickly obtained by neglecting the base current of the transistor and finding the voltage at the junction of R_1 and R_2. This voltage minus V_{BE} (approximately 0.2 volts) gives the voltage at the emitter. The emitter voltage is equal to the emitter current times the emitter resistor, R_3. By assuming the emitter and collector current equal, this method provides a good approximation of the collector current.

There are three major problems that must be considered in establishing the stability of a bias circuit. The emitter resistor is sometimes limited in value because the desired collector current causes too great a voltage drop for the available supply voltage. If the base circuit resistance is too low in an RC coupled amplifier, the input signal will be shunted by the base resistors. The DC power consumed by bias networks is often an important factor. Figure 7 shows typical bias circuits for several configurations. Notice that for a transformer coupled circuit, it is possible to avoid the shunting effect of the base resistances. Nonlinear elements such as thermistors or zener diodes are sometimes used for added stability. Proper bypassing of bias networks must be observed to avoid unwanted degeneration of the signal.

Audio and Video Amplifier Design

As was discussed earlier a common emitter low frequency amplifier gives the highest power gain for all values of load resistance. Since in transistorized amplifiers, power gain is usually required, the common emitter configuration is the most common. Untuned amplifiers may be classified in two groups, namely audio amplifiers (or fairly narrow band low frequency amplifiers) and video amplifiers, which amplify a very wide band of frequencies. Some important design considerations will be discussed for each type.

Audio Amplifiers

Audio amplifiers are usually RC coupled, direct coupled or transformer coupled. Each type of connection has its advantages and disadvantages. Direct coupled transistorized amplifiers require fewer components but present DC stability problems. No provisions for impedance matching are provided either. The stability problem may be overcome in resistance-capacitance RC coupled amplifiers, but mismatch is still a problem. The impedance of the bias networks can also be of great concern due to signal loading. Transformer coupled amplifiers give the best performance but are sometimes not possible because of the cost and/or size of the transformers. In direct coupled amplifiers, there is no limit on the low frequency response. The upper frequency is limited by the transistor. In RC amplifiers, the low frequency response is limited by the value of the coupling capacitors and the high frequency response by the transistor. Most practical transformer coupled amplifiers are limited at the low and high frequencies by the transformer. Partial bypassing of the emitter resistor is often used to extend the high frequency response. Some loss in low frequency gain will result.

In designing amplifiers for very low signal levels, noise may become a problem and transistors with specified noise figures should be used. The 2N207 transistor is a typical low noise audio transistor.

In communications circuits, audio amplifiers may be required to handle considerable power output. Class B push-pull connections are often used because more power output may be obtained for a given transistor dissipation rating. Figure 8 is a general circuit of this type. The amplifier consists of two transistors whose betas are matched operating as Class B common emitter amplifiers. R_T is provided for DC stability. Notice that it is common to both transistors, providing improved stability. R_1 and R_2 provide a slight amount of forward bias to the transistors to prevent "cross-over" distortion. Power supply requirements are not as great in a Class B amplifier since very little collector current flows when no signal is present. The average power of typical program material is only 1/10 of the peak power, thus permitting greater peak power.

A Class B push-pull amplifier is a large signal device thus making the input impedance of the transistors non-linear. For this reason, a low driving impedance (voltage source) is required for minimum distortion (R_{BB}). The power requirement also prevents impedance matching at the output. The maximum load impedance for an amplifier such as shown in Figure 8 may be calculated from

$$R_{Lmax} = \frac{V_{CC}^2}{2P_{o\ max}} \tag{8}$$

where V_{CC} is the DC supply voltage, R_{Lmax} is the maximum reflected load across half the primary winding, and P_{omax} is the maximum undistorted output power.

Maximum collector dissipation in a Class B amplifier occurs at approximately 40% of the maximum output.

Video Amplifiers

In the design of video amplifiers the circuit designer is concerned with obtaining power gain over a very wide frequency range. Since the low frequency end of the amplifier approaches zero, the bandwidth is taken as the upper frequency limit.

One of the basic parameters of a transistor for a video amplifier is f_T. The gain-bandwidth product of a single stage uncompensated video amplifier is approximately this parameter. The low frequency current gain of a transistor is $\beta(h_{fe})$; thus the bandwidth of a single uncompensated common emitter video amplifier is

$$BW \approx \frac{f_T}{\beta_o}. \tag{9}$$

This is the bandwidth which the stage will have if the signal source is a current source (high impedance) and the load impedance is low compared to the output impedance of the transistor; a practical condition in the interior stages of a cascaded video amplifier using common emitter connections. Note also that the BW depends on β_o. Therefore, it is possible to trade gain for bandwidth to some extent by varying β_o.

If the source impedance is reduced, the bandwidth will be increased somewhat. If the load impedance is increased, the bandwidth will decrease as shown in (10).

$$BW \approx \frac{f_T}{\beta_o} \frac{1}{1 + 2\pi f_T R_L C_C} \tag{10}$$

where R_L is the load resistance presented to the video amplifier stage and C_C is the collector-base diode capacity.

Ideally, the way to design a video amplifier would be to pick a transistor whose f_T equals the desired gain-bandwidth product. Since this is not always possible, a transistor having a higher low frequency gain is chosen and feedback is employed. Figure 9 shows how this is accomplished. G_{01} is the uncompensated current gain with a bandwidth of BW_1. The introduction of resistive feedback in the stage lowers the stage gain to G_{02} thus increasing the bandwidth to BW_2.

When two or more video amplifier stages are cascaded, a reduction in bandwidth may be expected. The reduction is given by

$$\frac{BW_{(n)}}{BW} = \sqrt{2^{\frac{1}{n}} - 1} \tag{11}$$

where $BW_{(n)}$ is the bandwidth of n stages cascaded, and BW is the bandwidth of a single stage (all individual stage bandwidths being equal), and n is the number of stages.

Figure 10 is a plot of a degradation factor for two video stages of unequal bandwidths.

Two transistor amplifiers have the advantage of more available gain, thus making the feedback more effective. Figure 11 is the circuit of a two stage video amplifier with interstage feedback.

The voltage rating and power dissipation of present day transistors is not sufficiently high to provide the voltage required by some devices. For this reason, a voltage doubler circuit is often used, providing a video output signal of almost twice the voltage rating of the

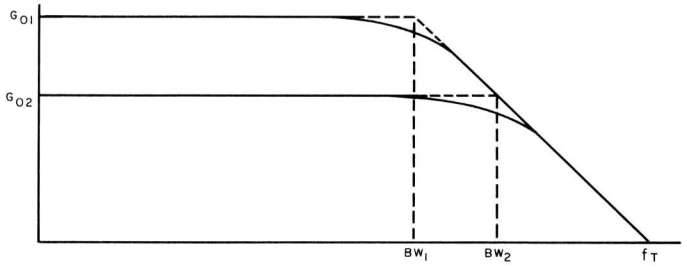


FIGURE 9 EXTENDING THE RANGE OF A VIDEO AMPLIFIER BY LOWERING THE CURRENT GAIN

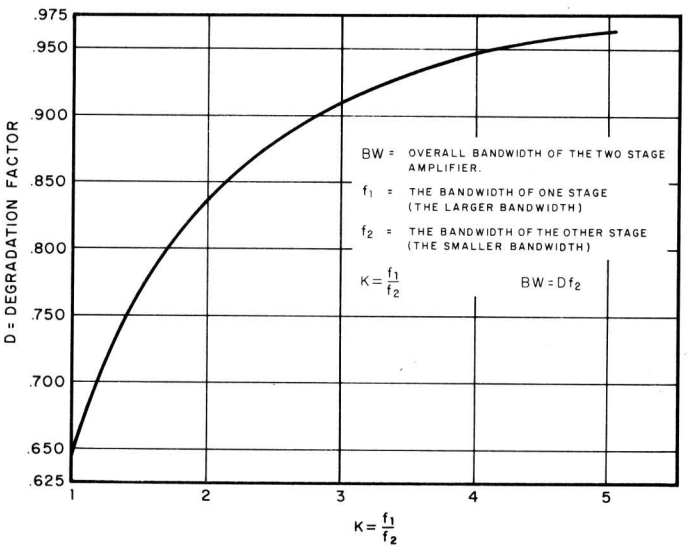


FIGURE 10 METHOD OF FINDING BANDWIDTH OF TWO STAGE AMPLIFIER WHEN BANDWIDTH OF INDIVIDUAL STAGES IS KNOWN

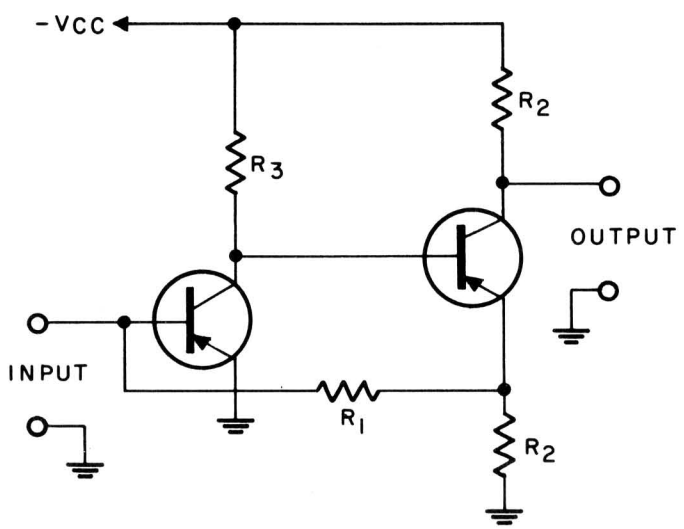


FIGURE 11 AC CIRCUIT OF A TWO STAGE VIDEO AMPLIFIER EMPLOYING INTERSTAGE FEEDBACK

transistor. Figure 12 shows the circuit of a typical voltage doubler video amplifier suitable for use in a TV receiver.

One additional consideration in video amplifier design is noise. As noted earlier, high frequency transistors have poor low frequency noise figures and low frequency transistors have poor high frequency noise performance. Therefore, if noise is important, the choice of the proper transistor is extremely important in wide band amplifiers. If low frequency performance is required, use the lowest frequency transistor possible which will still provide the proper bandwidth.

Common base and common collector amplifiers are often used in wide band applications where gain is of secondary importance. Both have wider natural bandwidths than the common emitter configuration. The common base has the widest natural bandwidth ($f_{\alpha b}$). The common collector is usually used for impedance matching.

Peaking networks may be used in video amplifiers. The simplest and most common is a partially bypassed emitter resistor. This provides frequency dependent degeneration and is very useful in many transistorized video amplifiers. Conventional shunt and series peaking with reactive elements may be used but they are often not very effective because the reactive elements in the transistor are separated from the external circuit by resistive elements.

Tuned Amplifier Design

Transistor Specification

The specification of transistors for tuned amplifiers can be divided into two basic categories. Low frequency (below the knee of the power gain versus frequency curve) and high frequency (above the knee of the curve). The low frequency design requires specification of current gain, input and output impedances, and feedback impedance of the transistor. The design then centers around the selection of the proper load and source impedance for a given gain and stability. This will be discussed in greater detail under the Design of Low Frequency Tuned Amplifiers.

The specification of high frequency transistors becomes much more complex. In order to adequately design a high frequency tuned amplifier circuit the following parameters of the transistor must be known and controlled.

1. Power Gain—The power gain must be guaranteed so that the proper number of stages can be chosen which will have adequate gain even with all low limit transistors.

2. Noise Figure—The noise figure is important in the early stages of a communications receiver because it limits the ultimate sensitivity of the receiver. It is also extremely important in receivers which use a diode mixer followed by an IF strip such as radar

and other UHF applications. Therefore, it is important that noise figure be guaranteed on transistors which are to be used in these applications. It is also important that the noise figure and gain be guaranteed at the same operating point because it is possible to optimize either the gain or the noise figure with a sacrifice in the other. It is impossible, however, in a practical receiver to adjust for both best gain and best noise figure simultaneously and the designer must settle for one or the other. By specifying gain and noise figure at the same point, the designer knows exactly what he can expect from the transistor under these conditions.

3. The resistive and reactive components of the input and output impedances must be known so that the circuit can be designed for the proper bandwidth, tuning range, loaded and unloaded Q's and so that the interstage networks may be designed to properly match the transistor for optimum gain.

4. The feedback elements within the transistor must be known so that proper neutralization networks can be designed. If the transistor is not neutralized, these elements will affect the gain and bandwidth of the system depending upon the amount of feedback from output to input. In the case of grounded base circuits too much feedback will cause the stage to oscillate.

Each of the parameters required for specifying high frequency transistors can be measured. However, some of the measurements are complex and time consuming. In addition, if a worst case design were made on specified parameters it might be impossible to fulfill the specific circuit requirements. This is because many of the parameters have opposite effects on circuit performance. What the circuit designer really wants to know is that the overall performance of the transistor and the circuit will be controlled. In order to provide the circuit designer with these controls a number of test philosophies for high frequency transistors have been developed. Three of these are described below with their advantages and disadvantages.

A. Typical performance

One of the earliest methods of specifying high frequency transistors and one that is still used today is that of giving typical performance of a switching transistor as an amplifier. This method has the advantage that one transistor may be used for both jobs. However, as noted earlier, it is not possible to optimize a transistor for both a switch and an amplifier. The more serious disadvantage of this means of specifying is that the circuit designer only has typical or design center values. He usually has no guaranteed limits on the four items noted earlier.

B. Matched, neutralized gain and noise figure

This method of specifying a tuned amplifier transistor has been used for some time. It is the best method of describing the potentials of the transistor. It gives an accurate measure of the power gain and noise figure and from this the f_{max} may be calculated. The main disadvantage of this system is that there is no control of the input and output impedances or the feedback capacity of the device except that provided by the range of the matching and neutralizing elements in the test circuit.

C. Functional testing

In order to overcome the disadvantage of the first two systems, Philco Corporation, Lansdale Division has adopted a philosophy of true functional testing. All of our new high frequency communications transistors for tuned amplifier design are being specified in circuits of this type. This method consists of testing the transistors in fixed matched, fixed neutralized and fixed biased circuits. The matching and neutralization are adjusted to perfectly match and neutralize the typical transistor. The bias is adjusted so that a transistor with a typical h_{FE} is operated at the optimum current. The only variable elements are the input and output tuning. By guaranteeing gain, bandwidth and noise figure, all measured at the same point (maximum gain), the circuit designer has control over all four of the prerequisites noted earlier. These circuits have been designed and built for several frequency ranges and experiments have shown that guaranteeing the performance of the transistor in a circuit of this type at one frequency guarantees its performance over a wide frequency range. For instance, specifying the 2N1742 at 200 mc assures satisfactory performance over the range of 50 to 300 mc. In addition to providing controls on all of the high frequency parameters, the use of conventional fixed biased networks also provides control of these parameters as the DC beta (h_{FE}) of the transistor varies from one transistor to another. This assures, in a practical circuit, that the operating point variations from transistor to transistor will not provide changes in high frequency performance greater than those shown in the specification.

Short Circuit Impedance Measurements

In order to provide a circuit designer with typical design center values of the resistive and reactive components of the input and output impedance, many manufacturers show short circuit impedance measurements on their data sheets. While there are other methods of presenting the typical impedance data such as h-parameters and y-parameters, the short circuit method is probably the easiest to use.

The short circuit measurements present the parallel equivalent resistance and reactance when looking into the transistor with the other two terminations ac short circuited. The reactive component is usually capacitive, however, at certain frequencies and con-

PHILCO COMMUNICA

Frequency	RF Amplifiers	IF Amplifiers	Mixers and Converters
0-20 KC			
20 KC-2 MC	2N1788 2N1785 2N1726 2N1267 2N773 2N393 2N344 2N346	2N1728 2N1747 2N1865 2N1866 2N1867 2N1790 2N1267 2N773 2N346 2N393	2N1727 2N1786 2N1789 2N1267 2N773 2N344 2N393 2N346
2-10 MC	2N1747 2N1867 2N1746 2N1267 2N773 2N346	2N1747 2N1746 2N1865 2N1866 2N1867 2N1267 2N773 2N346	2N1746 2N1747 2N1865 2N1866 2N1867 2N1267 2N773 2N346
10-30 MC	2N1745 2N1747 2N1867 2N502A 2N588 2N1270 2N776	2N1745 2N1866 2N1867 2N1747 2N502A 2N588 2N1270 2N776	2N1745 2N1866 2N1867 2N1747 2N502A 2N588 2N1270 2N776 2N346
30-70 MC	2N1742 2N1745 2N502A 2N1270 2N776	2N1745 2N1868 2N1742 2N502A 2N1270 2N776	2N1743 2N1745 2N502A 2N1270 2N776
70 to 400 MC	2N1742 2N502A	2N1742 2N502A	2N1743 2N502A
400 MC to 2 KMC	L5431	L5431	L5431

TIONS TRANSISTORS

Low-Level Oscillators	High-Level Oscillators	Multipliers	Audio or Video Amplifiers
			2N223 2N224 2N226 2N387 2N207 2N1129 2N535 2N597 2N600
2N1727 2N1786 2N1789 2N344 2N346 2N1267 2N773	2N1158A 2N1867 2N597 2N1267 2N773	2N1867 2N1267 2N773	2N597 2N600 2N1267 2N773 2N393 2N1748A 2N1749
2N1746 2N1786 2N1789 2N1267 2N773 2N346	2N1158A 2N1867 2N1267 2N773	2N1747 2N1867 2N1267 2N773	2N1267 2N773 2N1748A 2N1749 2N1745 2N1270 2N776 2N502A
2N1747 2N1867 2N502A 2N588 2N1270 2N776 2N346	2N1158A 2N1270 2N776	2N1744 2N1747 2N1867 2N1270 2N776 2N1158A	2N1745 2N502A 2N1742 2N1270 2N776
2N1744 2N502A 2N1270 2N776	2N1158A 2N1270 2N776	2N1158A 2N1744 2N1270 2N776	2N1742 2N502A 2N1270 2N776 2N769
2N1744 2N502A	2N1158A	2N1744 2N1158A 2N502A	2N1742 2N502A 2N769
L5431	L5431	L5431	2N769 L5431

nections it may be inductive. Inductive reactance is usually represented on these data sheets as negative capacitance. This indicates an inductance whose reactance is equal in magnitude to the reactance of the negative capacitance shown.

The short circuit measurements provide a very accurate method of determining the impedances for neutralized amplifier design. One simply matches to the resistive component of the short circuit impedance and considers the reactive component in determining the LC ratio of the tuned circuit. While these impedance measurements are not completely accurate for unneutralized amplifiers, they do provide a reasonable approximation and are useful for most designs.

Low Frequency Tuned Amplifier Design

As was mentioned earlier, the neutralization of tuned amplifiers at low frequencies becomes complex and unreliable. Mismatch is therefore used for stabilization. Using the general circuit outlined in Figure 13, the desired DC operating point is chosen and then the transformer is designed. In designing for mismatch, a major portion of the load presented to the transistor must be contributed by transformer insertion loss. This is necessary because the very high output impedance of a transistor preceding a transformer can not reflect a low impedance to the following transistor and at the same time permit the second transistor's input impedance to load the first transistor; or, it is impossible to mismatch on the low side on both primary and secondary without the transformer contributing most of the load. Also by having the transformer loss resistance great, variation in loading due to variations of transistor parameters is less of a problem. It may seem that considerable power gain is sacrificed for the desired stability, but with present day transistors the useful power gain is more than sufficient for most applications.

There are any number of combinations of load and source resistances in an amplifier for a given stability, however, equations have been derived which give the optimum values for maximum useful transducer power gain and minimum variation of gain with change in h_{fe}. The equations[2] for the optimum load and source resistance are:

$$
\begin{aligned}
O &= R_g^5 (A r_{i2} - k\lambda_2)(2R_1 + r_C) \\
&+ R_g^4 \{2r_{i2}(2R_1 + r_C)(A r_{i2} + k\lambda_2) - r_{i1}(R_1 + 2r_C)(A r_{i2} - k\lambda_2)\} \\
&- R_g^3 \{r_{i1}(A r_{i2} - k\lambda_2)[r_{i1}(4R_1 + 3r_c) - 4R_1 r_{i2}] + k\lambda_2 r_{i2}[3r_{i2}(2R_1 + r_c) + 4R_1 r_{i1}]\} \\
&- R_g^2 \{r_{i1}^2 (A r_{i2} - k\lambda_2)(R_1 r_{i1} + 2r_c r_{i2}) + k\lambda_2 r_{i1} r_{i2}[2r_c(r_{i2} - r_{i1}) + 9R_1 r_{i2}]\} \\
&+ R_g (k\lambda_2 r_{i1}^2 r_{i2}^2)(r_c - 4R_1) \\
&- 2K\lambda_2 R_1 r_{i1}^3 r_{i2}^2
\end{aligned}
\tag{12}
$$

and

$$
R_L = \frac{k\lambda_2 r_o (R_g + r_{i2})}{R_g (A r_{i2} - k\lambda_2) - k\lambda_2 r_{i2}} \tag{13}
$$

The symbols are defined in Table I.

The gain is optimized for the lower limit of h_{fe} and the stability factor is established using the high h_{fe} limit. The load and source resistances calculated from these equations provide the maximum transistor plus transformer gain for a given stability.

High Frequency Tuned Amplifier Design

The design of tuned amplifiers at high frequency lends itself very well to matched neutralized circuits. Since, for a neutralized amplifier, the input and output impedances are approximately equal to the short circuit input and output impedances of the transistor, the recommended design procedure for such stages is as follows: (Refer to Figure 14)

1. Select the operating point. The manufacturer usually specifies the operating point for optimum gain. In the case of Philco, other points may be satisfactory, however, with some sacrifice in performance.
2. From curves of short circuit input and output impedance, estimate the input and output impedance at center frequency.
3. Select the turns ratio of the input transformer to match the source to the parallel resistive component of the input impedance. Any mismatch will lead to a reduction in stage gain.
4. Select the LC ratio of the input circuit to produce the desired interstage Q (bandwidth). Adjustment of bandwidth through the use of loading resistors will result in reduced stage gain. (Include the parallel part of the short circuit C_{in} when calculating the LC ratio.)
5. Select the turns ratio of the output transformer to match the parallel resistive component of the output impedance to the load. Select the LC ratio as in Step 4. Wind a few additional turns on the primary (neutralization winding) as shown in Figure 14.

2. For a detailed discussion of these equations and also equations relating to transformer design refer to Application Lab Report 685

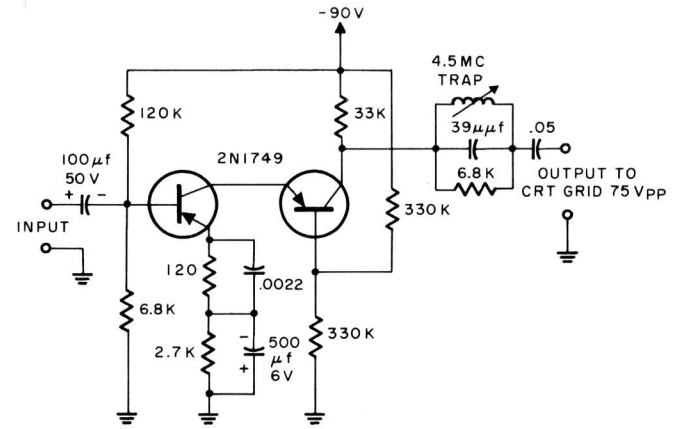


FIGURE 12 TYPICAL VOLTAGE DOUBLER TV VIDEO AMPLIFIER

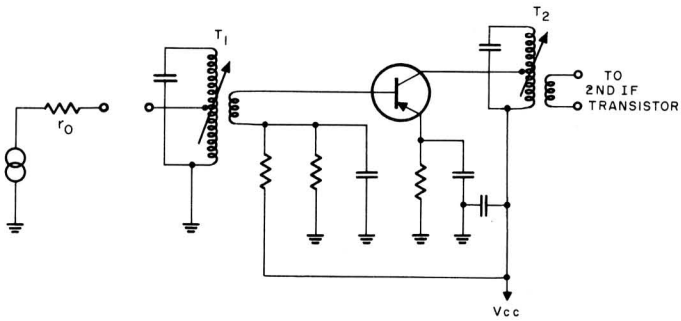


FIGURE 13 BASIC LOW FREQUENCY TUNED AMPLIFIER CIRCUIT

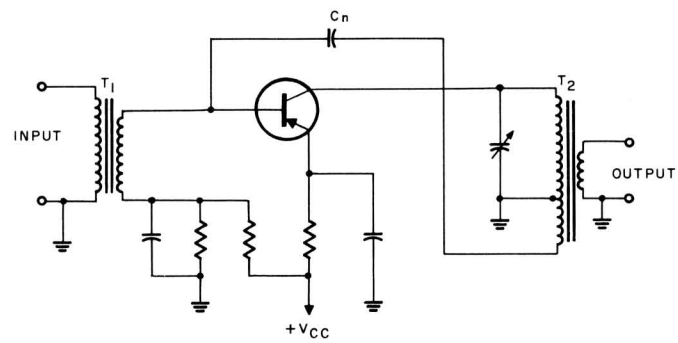


FIGURE 14 BASIC HIGH FREQUENCY TUNED AMPLIFIER CIRCUIT

A	=	$\omega C_f g_m r_o$
C_f	=	collector to base feedback capacitance
g_m	=	transistor transconductance
k	=	constant whose value depends on number of stages in amplifier (2, 1 and 0.767 for one, two and three stage amplifiers, respectively)
r_c	=	output resistance of preceding stage
R_g	=	source resistance feeding transistor
r_i	=	transistor input resistance for which gain is optimized
r_{i1}	=	transistor input resistance at low end of beta range
r_{i2}	=	transistor input resistance at high end of beta range
r_o	=	output resistance of transistor
λ	=	stability factor
λ_1	=	stability factor using lowest beta unit
λ_2	=	stability factor using highest beta unit (usually assumed to be 0.2)
ω	=	2π x center frequency of amplifier

TABLE I LIST OF SYMBOLS

6. Select the neutralizing capacitance using the turns ratio selected in Step 5 and the collector-base capacity of the transistor. (This value will neutralize the stage against feed-through due to the transistor.) If there is appreciable feed-through due to the circuit layout, socket coupling, etc., this value must be modified accordingly. Keep in mind that the neutralization signal is basically a voltage feedback. Thus, the value of the neutralization capacity can be calculated directly if the turns ratio and coupling coefficient of the transformer are known along with the feedback capacity of the transistor.
7. Good high frequency construction techniques should be used including isolation of input and output, common point grounding, etc.
8. The design of amplifiers in the region of the knee of the power gain versus frequency curve may require mismatch for stability. In general, any amplifier with over 30 db gain per stage is approaching the unstable region of the transistor. In amplifiers whose gain is greater than this, some mismatch is usually suggested. Fixed neutralization is usually not practical in stages where the gain exceeds 30-35 db per stage.

Multipurpose Functions

Occasionally a transistor may be required to provide more than one function in a circuit. Such circuits are common in superregenerative receivers, reflex amplifiers and IF amplifiers for AM-FM receivers. In selecting a transistor for a multi-purpose function, it is necessary to consider the transistor requirements for all of its intended applications. For example, in specifying a transistor for an AM-FM IF amplifier which will operate at 455 kc on AM and 10.7 mc on FM, it is necessary that the transistor provide excellent performance at both of these frequencies. Therefore, the low frequency current gain and impedance must be specified for 455 kc and its high frequency power gain must be specified for 10.7 mc. Merely guaranteeing the performance of a transistor in the high frequency region will not guarantee its performance in the low frequency region, nor will specifying a transistor for a tuned amplifier necessarily insure good performance in an untuned amplifier. Figure 15 shows a circuit of an AM-FM IF amplifier which uses transistors that have been specified for the dual purpose application.

AGC Characteristics

In most communications receivers there is a sufficiently wide range of input signals so that some method of automatic gain control is required. Present day transistors can be gain controlled in two ways. The first of these, Reverse AGC, is a conventional method with the gain reduction occurring as a result of the reduction of collector current and extreme mismatch. The second, Forward AGC, is a gain control method which results from a reduction in gain as the collector to emitter voltage is lowered. The gain falls with col-

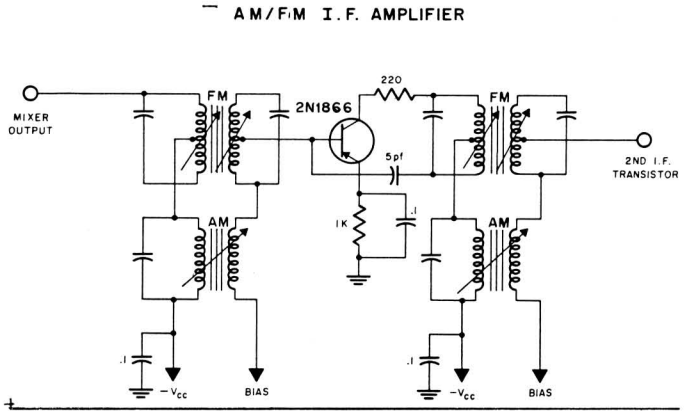


FIGURE 15 AM/FM I.F. AMPLIFIER

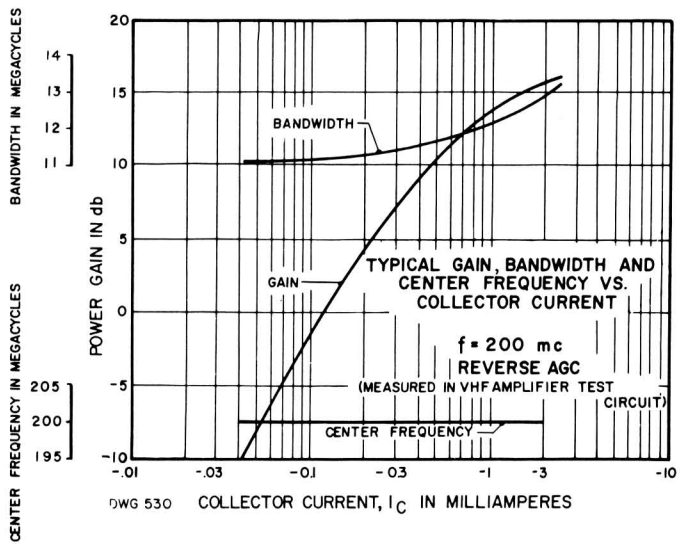


FIGURE 16 REVERSE AGC CHARACTERISTICS 2N1742

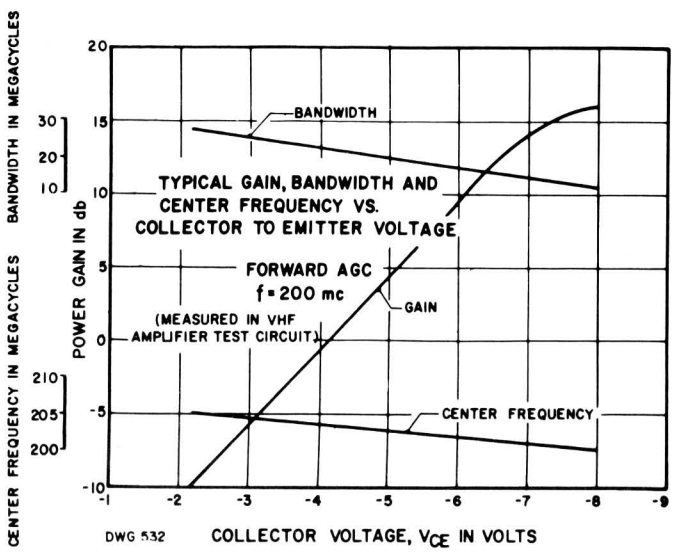


FIGURE 17 FORWARD AGC CHARACTERISTICS 2N1742

lector to emitter voltage on all transistors, however, the MADT is the only device specifically designed to make use of this characteristic for gain control purposes. In other transistors the gain falls much too rapidly to make it useful as a method of AGC. Each of these methods will now be discussed in more detail.

Reverse AGC

Figure 16 shows a curve of the power gain as a function of collector current for the 2N1742 MADT. This is typical of the reverse AGC action most transistors exhibit. This phenomenon exists at all frequencies although it is usually not used below 100 kc. As a rule of thumb you can expect the gain reduction per transistor to be about 10 db more than the stage gain of the device at that frequency. Another way of saying this is that the gain of the stage may be varied from the maximum gain of the stage to about —10 db. In obtaining the curve of Figure 16 the amplifier was tuned at the normal operating current of about 2.5 ma and the collector current was changed by applying a positive going voltage to the base of this PNP transistor. The circuit was not retuned during these measurements thereby simulating the AGC action in a practical circuit. Also shown in Figure 16 is the variation of center frequency and bandwidth over this current range. Notice that there is very little change in center frequency and a relatively small change in bandwidth with reverse AGC.

Forward AGC

Figure 17 shows a curve of power gain in db versus collector to emitter voltage on the 2N1742 MADT. This type has been specifically designed as a VHF amplifier and the forward AGC characteristic has been built into the device. Such a falloff of gain versus voltage would be extremely undesirable in the switch. This again indicates the flexibility of the Precision-Etch* process in optimizing transistors for switches, amplifiers, oscillators, etc. The circuit of Figure 18 shows how the forward AGC action is obtained. Notice that a bypassed resistor is included in the collector circuit. The value of this resistor is usually between 1000 and 3000 ohms. Its value will depend upon the supply voltage used, the value of the emitter stabilizing resistor and the current at which the particular transistor reaches maximum gain. To obtain forward AGC action the base is driven more negative. This increases the collector current causing a drop across R_C and a reduction in collector to emitter voltage. In designing a circuit for forward AGC action the following steps should be adhered to:

1. Determine the current for optimum gain (I_{Cmax}).
2. Determine the value of the emitter stabilizing resistor (R_E). Remember that the changing current in the transistor will change the voltage drop across this resistor and will add to the total AGC voltage which must be applied to the base of the transistor. For example, a 500 ohm emitter resistor and a col-

*Trademark Philco Corp.

lector current which changes from 2 to 6 ma from maximum to minimum gain (a total change of 4 ma) will cause a change in voltage across the emitter resistor of 2V. Therefore, it will be necessary to supply at least a 2V change in AGC voltage to the base to accomplish this change in current.

3. Determine the lowest collector to emitter voltage (V_{CEmin}) that the transistor can operate at and still remain above the knee of the power gain versus voltage curve.
4. If the supply voltage (V_{CC}) is fixed, the value of the collector resistance (R_C) can be chosen simply by

$$V_{CC} = V_{CE(min)} + (I_{Cmax}) (R_E + R_C) \qquad (14)$$

5. $R_C + R_E$ must be large enough so that the total dissipation of the transistor is not exceeded over any portion of the AGC range. This can be calculated from the DC operating conditions.
6. It is sometimes desirable to use a slightly higher supply voltage and also a slightly higher R_C than normal with forward AGC. It is obvious that the speed of the AGC action can be readily controlled by varying the sum of $R_E + R_C$.

The curve of Figure 17 shows that there is somewhat more center frequency and bandwidth shift with forward AGC than there is with reverse AGC. Note, however, that the bandwidth shift is in the opposite direction.

Overload Performance

One of the most serious problems encountered in transistorized receivers is that of overload and cross modulation distortion. This is the chief reason for using forward AGC. Figure 19 shows a curve of the typical overload level as a function of the power gain for the 2N1742. The overload level is defined as that signal input which causes a specified amount of distortion in the output. Notice that when the gain is reduced by reverse AGC techniques the transistor is able to handle less and less signal without distorting. This is opposite to the desired result because as the gain is reduced in the transistor the magnitude to the incoming signal is becoming larger. Under forward AGC action the desired result does occur and at the extremities of the curve forward AGC will handle at least 100 times more power input than reverse AGC for the same level of distortion.

Therefore, in designing communications circuits, it is recommended that forward AGC be used in those stages where strong signals are encountered such as the RF and first IF stages. In later stages in the receiver either type of AGC may be used. If extreme control of bandwidth and center frequency is required, then it may be necessary to use reverse AGC or to use forward AGC and heavily swamp the transistor impedances.

Sometimes the fact that the bandwidth shifts in opposite directions with the two types of AGC is used in designing amplifiers. The compensating action is such that the overall bandwidth remains reasonably constant.

Mixer and Converter Design

Several general comments can be made concerning the design of high frequency mixers and converters. In general, the power gain and noise figures are about the same regardless of whether a mixer is used with a separate local oscillator or whether the circuit uses a self oscillating mixer (converter). However, converters are considerably more susceptible to variations in operating point and to the problems of oscillator pulling with changes in signal level. Therefore, one may conclude that, in general, converter circuits can be designed over most of the frequency range where mixers are usually used providing one is willing to accept some degradation in stability.

Two types of mixer and converter circuits are in common use. These are: first, the circuit using base injection of the oscillator signal and second, a circuit using emitter injection of the oscillator signal. Experimental evidence shown in Figure 20 indicates a slight preference for emitter injection at frequencies above 100 mc. Usually economics and circuit layout dictate the choice of emitter or base injection.

The gain of a mixer or converter depends upon both the incoming signal and the IF frequency. In general, the gain of a mixer can be approximated by assuming the device to be a diode mixer with about 15 db loss followed by an IF amplifier whose gain may be calculated by knowing the f_{max} of the transistor. The loss term is actually dependent upon the RF signal but is usually between 15 and 20 db. The gain is also dependent upon the oscillator injection power as shown in Figure 21. Notice, however, that the gain is relatively independent of injection power above 1 mw. Sometimes it is more convenient to think of injection power in terms of voltage. In this case an injection voltage of about 150 mv is a reasonable number. Mixers and converters usually operate at somewhat lower current for optimum conversion action than does the same transistor as an amplifier. In the low frequency region collector currents of about .7 ma are usually the best. At higher frequencies, currents of 1 to 1.5 ma usually provide optimum performance. Figure 22 shows the variation of conversion gain with collector current for the 2N1743.

The noise figure of converters and mixers is also dependent on operating point and oscillator injection power. Figures 23 and 24 show the variation of noise figure with current and injection power. Notice the noise figure rises with current and decreases with injection power. This is fairly typical of most mixers and converters. Therefore, in designing mixers and converters, it is desirable to know the variation of gain and noise figure with injection power and operating point. For a unit such as the 2N1743, it can be seen that a good operating point to conserve injection power would be at a collector current of about 1 ma and an injection power of 1 to 2 mw.

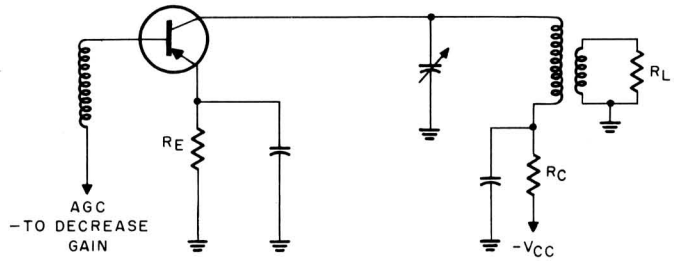


FIGURE 18 FORWARD AGC CIRCUIT

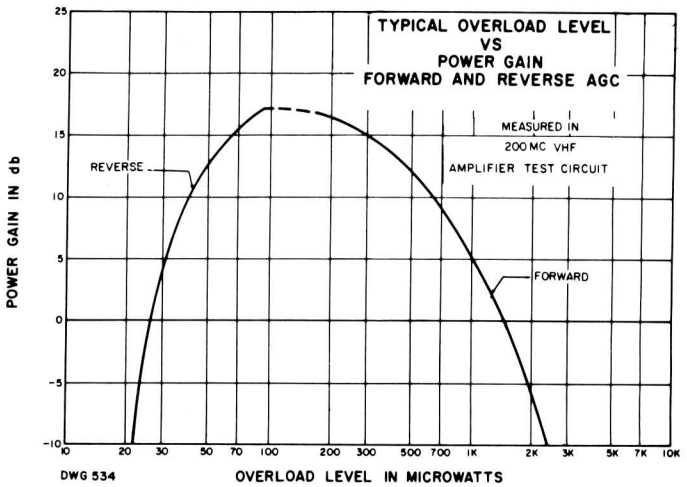


FIGURE 19 OVERLOAD PERFORMANCE 2N1742

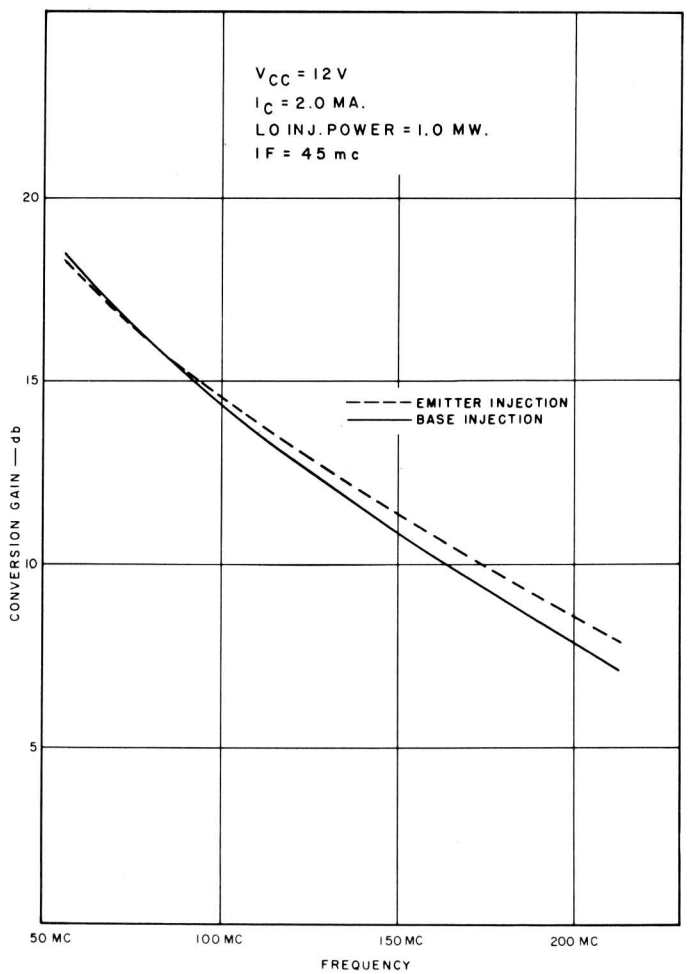


FIGURE 20 CONVERSION GAIN VS FREQUENCY 2N502

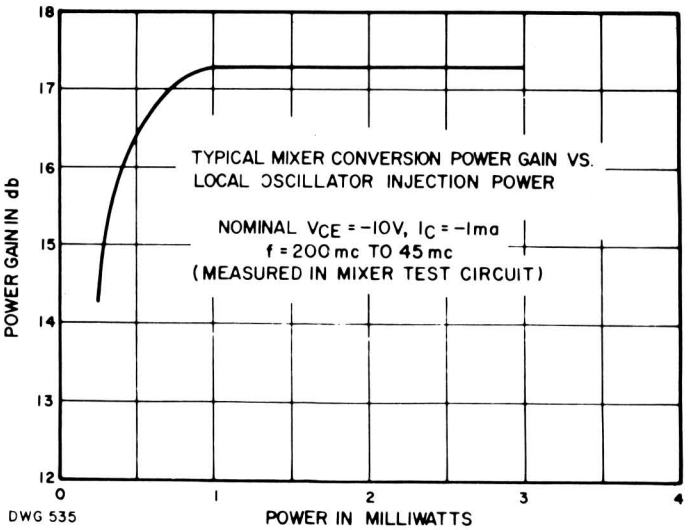


FIGURE 21 CONVERSION GAIN VS INJECTION POWER 2N1743

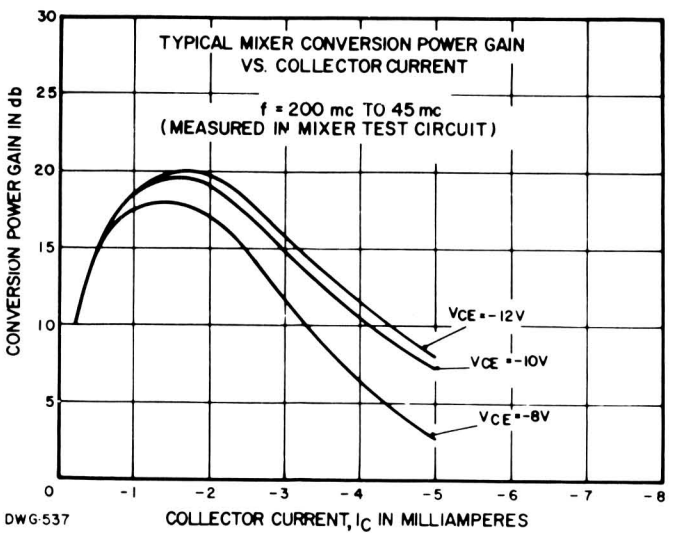


FIGURE 22 CONVERSION GAIN VS COLLECTOR CURRENT 2N1743

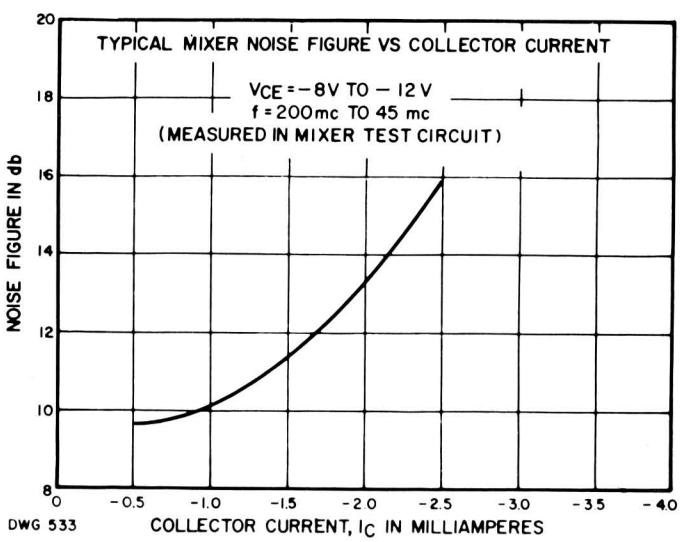


FIGURE 23 CONVERSION NOISE FIGURE VS COLLECTOR CURRENT 2N1743

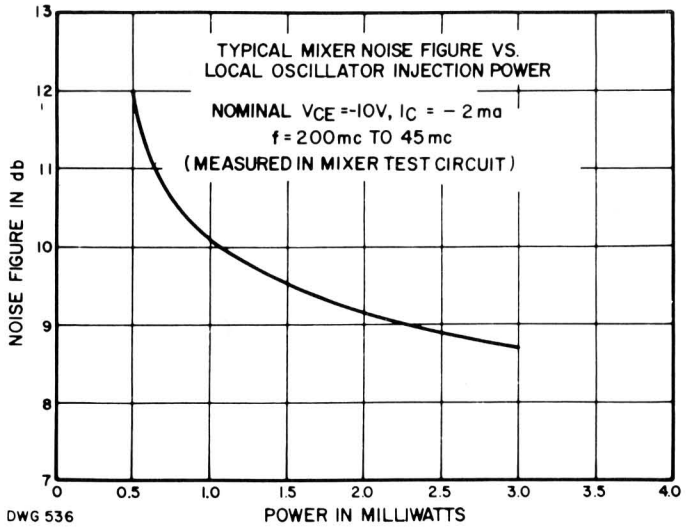


FIGURE 24 CONVERSION NOISE FIGURE VS INJECTION POWER 2N1743

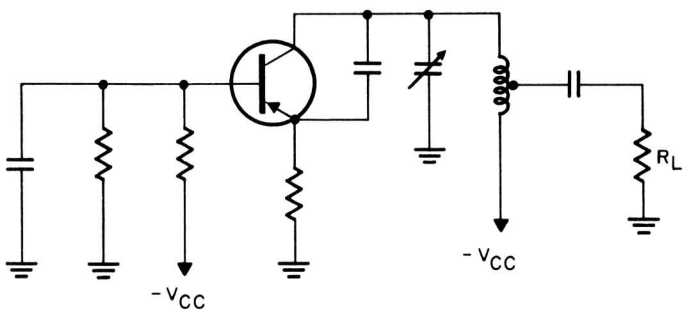


FIGURE 25 TYPICAL COMMON BASE OSCILLATOR

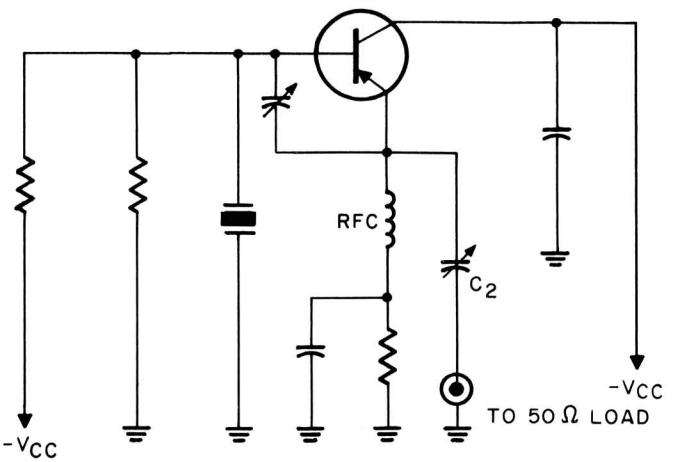


FIGURE 26 UNTUNED CRYSTAL OSCILLATOR

Experiments have shown at high frequencies that there is not necessarily good correlation between the operation of a transistor as a mixer and converter and its operation as a RF amplifier. For this reason, we specify transistors in functional circuits which have guaranteed mixer performance.

In the design of mixer and converter circuits it is extremely important that the impedance between the base and emitter be low at the IF frequency. This applies to both common base and common emitter mixers and converters. Often the gain of the mixer will appear to be low. When this happens, insert a series trap tuned to the IF frequency between the base and emitter. If the gain increases, then there is considerable degeneration occurring in the base emitter circuit. This may be fixed by inserting the series trap as part of the design or in the case where a tapped transformer is used, the base can be tapped low enough on the transformer so that this small inductance is a low impedance at the IF frequency.

Oscillator Design

For most high frequency oscillators the conventional common base configuration shown in Figure 25 is most useful. The common base circuit is naturally regenerative at these frequencies and the addition of slight additional collector to emitter feedback capacity will cause the transistor to oscillate. For most transistors this method works well above 50 mc. A means should be provided to match the oscillator output to the load.

For frequencies below 50 mc, the phase shift in such a circuit may not be adequate to provide efficient operation. In this frequency range it may be necessary to tap the feedback capacity down on the collector tank circuit.

Transistorized crystal controlled oscillators may be made in any number of configurations with the crystal forming a part of the feedback network. In general, the crystal will absorb about 1 to 2 mw of power and for this reason the output from a crystal controlled oscillator will be about this much less than the output from an uncontrolled oscillator. It is also possible to build crystal controlled oscillators which do not have an LC tuned circuit external to the oscillator. Experience has shown that a common collector circuit such as shown in Figure 26 provides the best performance in this type of circuit.

As a general rule of thumb, one can expect the efficiency of a high frequency oscillator to increase at about 15% per octave as the frequency is reduced. Operation as an oscillator, however, is very dependent upon the r_b' of the transistor, with the low r_b' units having the highest efficiency. Therefore, it is necessary that transistors be optimized to provide good high frequency oscillator performance. For this reason, Philco transistors are specified in oscillator circuits with a guaranteed minimum output power.

Multiplier Design

The use of transistors as high frequency multipliers

is a subject which is not well understood. However, certain transistors do make good multipliers and, in general, those transistors which are good oscillators are also good multipliers. However, experimental evidence indicates that this is not always true. The circuit of Figure 27 shows a typical multiplier operating from 20 mc to some harmonic of 20 mc. The chart below shows the approximate value of the emitter resistor R_E for each harmonic. In designing the circuit, R_E should be varied to optimize its value for maximum power output.

Harmonic	R_E ohms
2nd	470
3rd	820
4th	1100
5th	1300

A good rule of thumb to use in calculating the output power from a multiplier is given below:

$$P_{out} \approx \left(\frac{1}{n}\right)^2 (P_{GM}) \qquad (15)$$

where n is the harmonic to which the output is tuned and P_{GM} is the maximum class C power gain of the device when operated as a straight through amplifier at the fundamental frequency.

Transmitter Output Stage Design

Recently a number of transistors have become available which will provide a considerable amount of output power at high frequencies. The design of high frequency, high power output stages is best accomplished by trial and error. Figure 28 shows a sketch of a high frequency output stage. Experience has shown that the coupling system used on the input, which results in extremely tight coupling from the generator to the transistor, works best in this type of circuit. First, more efficient coupling of the generator power to transistor is accomplished and second the loading on the transformer prevents sudden transients from damaging the transistor.

The emitter resistor is adjusted for optimum conditions. Actually as the emitter resistor is increased, the transistor is driven further into the class C region. While this improves the efficiency, it also decreases the power gain of the amplifier. Therefore, a compromise must be made between efficiency and gain.

Insertion of the modulation transformer in the emitter circuit as shown also appears to help prevent transients which might damage the transistor. In the design of the output circuit, it must be remembered that there is only one combination of supply voltage and load resistance which will give maximum gain and output power. This is because the load must be matched to the transistor for optimum gain. However, maximum power output occurs when twice the supply voltage appears across this load. Therefore, only one load resistance will match the transistor and once this is fixed only one supply voltage will allow the transistor to swing over its entire load line. This optimum supply voltage on many present day transistors occurs between 15 and 20 volts. Thus the transistor voltage rating must be at least twice this and if collector or emitter modulation is used, as shown in Figure 28, the transistor voltage must be still higher depending upon the percentage modulation.

Experience has indicated that the common emitter configuration appears most stable and most efficient for these output stages. When additional power is required, our experience indicates that better operation is obtained with two transistors in parallel operating through two separate emitter resistors for stability. The two transistors in parallel appear to be more efficient and provide more gain than the same two transistors connected in either a push-pull or push-push type circuit.

Temperature and Life Considerations

Temperature

From the viewpoint of life and satisfactory operation, the temperature of the transistor junction is probably the most important single factor. When designing transistor circuits, every attempt should be made to keep the junction temperature as low as possible. This may be accomplished in two ways. First, design the circuit to operate at as low an ambient temperature as possible. Second, do not dissipate more power in the transistor than required for proper operation. Experimental evidence indicates that the expected transistor life is approximately doubled for every 10°C that the junction temperature is lowered.

Leakage currents are the most sensitive to temperature changes, particularly I_{CBO} which approximately doubles for every 10°C increase in temperature. In designing bias networks, the change in I_{CBO} with temperature should be considered so that the correct operating point is maintained over the temperature range.

Wide variations of ambient temperature do not affect high frequency performance appreciably if the DC conditions do not change. Figure 29 shows the relative power gain of a 2N1747 at 10.7 mc as the transistor temperature is varied from −60°C to +100°C. For this wide range of temperature, there is only a 3 db change in gain. Note that only the ambient temperature of the transistor was changed. Designers sometimes experience large variations in gain when the complete circuit is changed in temperature. If this happens, determine in separate tests whether the transistor characteristics are changing, or those of the other components.

Life

Life tests have shown that the parameters which affect the high frequency performance of the transistor do not materially change with life. It has also been shown that if the static characteristics of the transistor, that is, I_{CO}, β, etc., do not change, then the noise figure, gain and impedance of a transistor operating in a typical high frequency circuit will

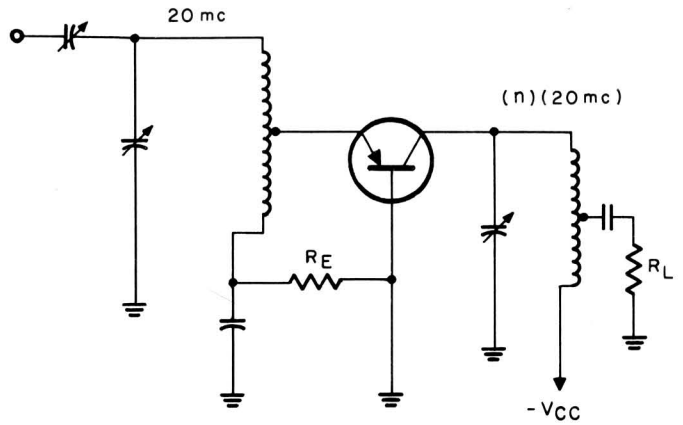


FIGURE 27 TYPICAL MULTIPLIER CIRCUIT

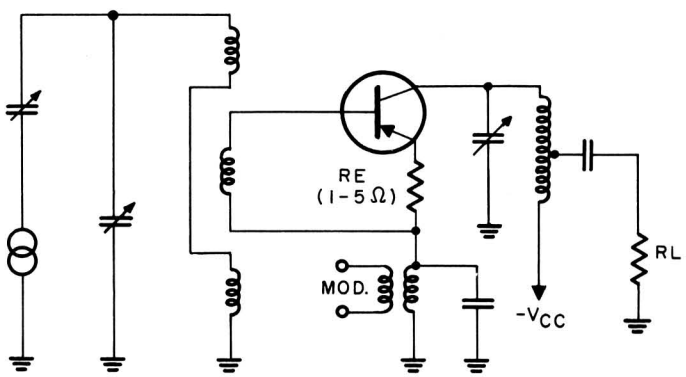


FIGURE 28 TRANSMITTER OUTPUT STAGE

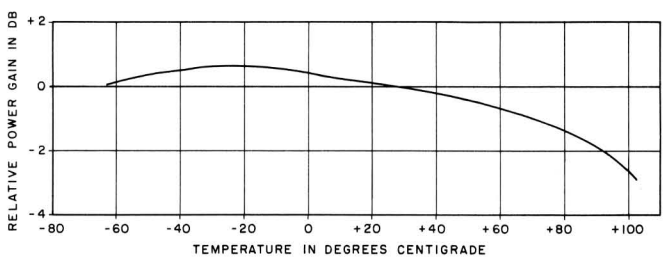


FIGURE 29 2N1747 TEST CIRCUIT
RELATIVE POWER GAIN VS TEMPERATURE
AT 10.7 mc. O DB = 28.8 DB

not change. If the static characteristics do change, they may affect the operating point and cause the transistor bias, impedance levels, etc., to change causing a small change in the actual performance of the circuit. Based on the tests that have been conducted, these changes would not affect the performance of the transistor in a typical circuit until such time as the transistor had reached what would normally be considered an end of life condition. It can, therefore, be concluded that normal static life test measurements are valid for the high frequency performance of a transistor in a practical circuit, and that as long as the static characteristics do not reach their normal end of life condition, the transistor will perform at or near its original performance in its circuit.

SUMMARY

The design of transistorized communications circuits is a complex and difficult job. However, there are a number of basic considerations which should be investigated before any circuit design is attempted. These are summarized below:

1. Make certain that the transistor is designed and specified for the particular mode of operation desired.
2. Select a transistor with adequate frequency response to provide the required stable gain, power, etc.
3. Select adequate voltage ratings and design the circuit so the transistor rating is never exceeded.
4. Choose other low frequency parameters to assure stable bias and high temperature operation.
5. Design the circuit to operate at the operating point specified by the manufacturer whenever possible.
6. Provide stable bias networks to allow for beta, I_{CBO} and temperature changes.

In each of the recommendations noted above the implication is that the proper transistors must be chosen for the job. The chart shown on pages 10 and 11 is intended to be a guide to help the designer choose the proper transistor. The Philco communications line has transistors designed and specified to fill virtually every communications socket. Additional design information and application notes describing specific circuits are available for most communications applications.

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