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"A SURVEY OF SOME CIRCUIT APPLICATIONS OF THE SILICON CONTROLLED SWITCH AND SILICON CONTROLLED RECTIFIER".

Bulletin D420-02 - 12-59

SOLID STATE Products, Inc.
ONE PINGREE STREET • SALEM, MASSACHUSETTS
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CONTENTS

1 INTRODUCTION

The PNPN Silicon Controlled Switch is an active switching element with characteristics similar to those of a gas thyratron. That is, it will remain in a non-conducting or "off" state until turned on.

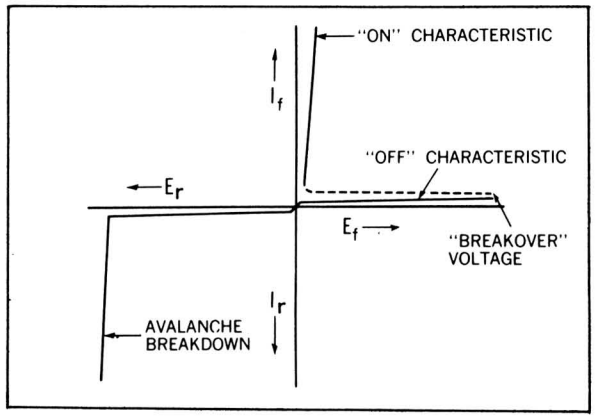

Fig 1 Typical E-I curve

or "fired" by a low level control signal It will then remain on without the need for sustaining control signal The Controlled Switch is turned off by reducing its anode current to below the "dropout" level Its E-I characteristic is shown in Figure 1

The Controlled Switch (CS) is similar to the Silicon Controlled Rectifier (SCR) in both physical construction and theory of operation The CS however, has a much greater firing sensitivity It is therefore useful in many low level input applications that are not within the capability of the Controlled Rectifiers

Much of the information presented in the following sections applies to both the CS and SCR.

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2 COMPARISON TO OTHER SWITCHING ELEMENTS

The CS can complement as well as supersede many other switching elements such as thyratrons, tubes, magnetic amplifiers, relays, mechanical switches, transistors and unijunction transistors

In comparison with mechanical devices such as relays, the CS has the advantages of no moving parts, miniature size, high speed operation, billions of switching cycles without maintenance or wear out, ability to withstand high shock and vibration, no contact "bounce" or arcing; high sensitivity, and low hold-in current

The CS can be used in place of gas thyratrons in many applications In addition to its obvious advantages of smaller size, greater ruggedness, and elimination of filament, it is also free of jitter, firing instability, and aging effects common in thyratrons Its forward voltage drop is many times lower resulting in much higher operating efficiency

Frequently, the CS can be used to advantage in place of conventional transistors in applications requiring high gain, high peak current, or high voltage ratings Current gain up to 50,000 is practical Peak currents of 20 amps can be achieved for short duration, low duty cycle pulses Voltage ratings extend to 200 volts The "latch on" property of the CS can simplify many D C circuits Since the output waveshape from a CS is independent of the input wave shape, it can operate reliably from "sloppy" pulses that would require special shaping to drive a transistor

Associated with the high peak current and high voltage ratings, is a turn-on time in the region of 1 microseconds which makes the CS useful in pulse modulators for radar and beacon transmitters

Unlike the transistor, the saturation resistance of the CS decreases as the anode current increases Input requirements for turn-on are independent of anode current, even at peak current levels of 20 amps Thus switching circuit performance actually improves at higher operating currents

The unique properties of the CS now permit the "semiconductorizing" of many circuits that up to now could not practically be transistorized

It is also useful to compare the CS with the unijunction transistor and the four layer diode Although these latter two devices operate on quite different principles they are similar in two respects Both fire when a "breakover" or "peak point" voltage has been exceeded, and in both, the control and load circuits are in common In the CS, control and load circuits are independent Firing voltage is much lower and more closely controlled The CS circuits therefore offer much greater design flexibility Circuit firing point can be precisely set within close tolerance without the need for special selection. The saturation voltage of the CS is significantly lower than that of the unijunction transistor, and current handling capacity is much greater

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3 ELECTRICAL CHARACTERISTICS

Operation

The operation of the CS can be best understood by considering the analogy of two silicon transistors, an NPN and a PNP connected as shown in Figure 2C

The collector of the NPN drives the base of the PNP and the collector of the PNP drives the base of the NPN This positive feedback loop has a gain equal to $\beta_1\beta_2$ the product of the current

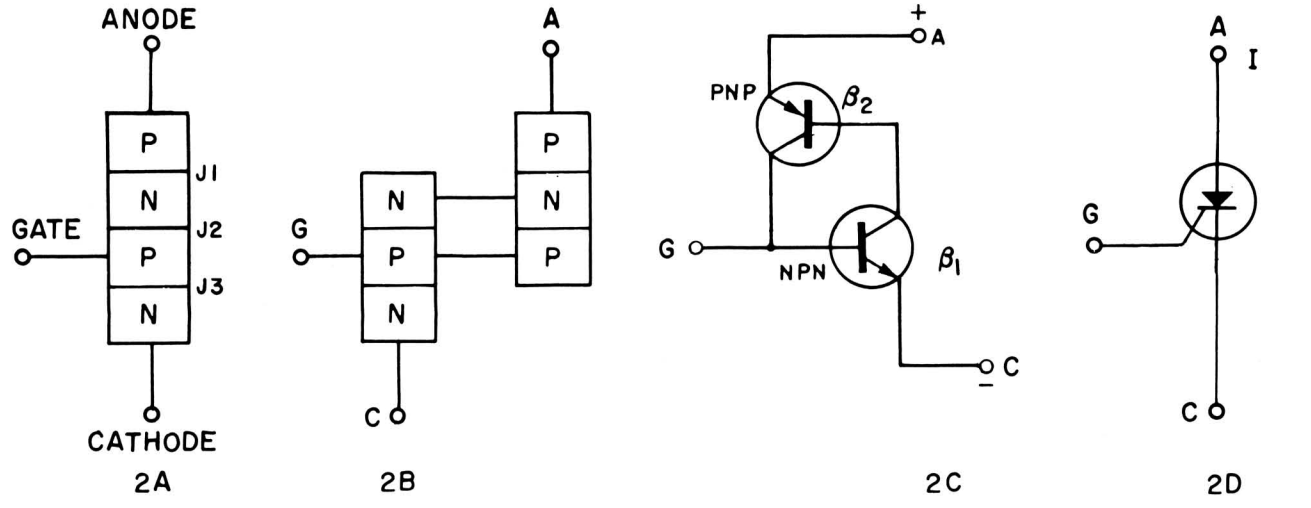

Fig 2

gains of the two transistors The circuit is stable as long as $\beta_1 \beta_2$ is less than unity but becomes self-regenerative when the loop gain reaches unity

With a small negative current applied to terminal G, the NPN transistor is biased off and the loop gain is less than unity The only current that can flow between output terminals A and C is the cut-off collector current of the two transistors Consequently the impedance between A and C is very high.

When a positive current is applied to terminal G, the NPN transistor is biased on, causing its collector current to rise Since the current gain of the NPN β_1, increases with increased collector current, a point is reached where the loop gain equals unity and the circuit becomes regenerative Collector current of the two transistors rapidly increases to a value limited only by the external circuit Both transistors are driven into saturation and the impedance between A and C is very low The positive current applied to terminal G which served to trigger the self-regenerative action is no longer required since the collector of the PNP transistor supplies more than enough current to drive the base of the NPN The circuit will remain in the "on" state until turned "off" This is accomplished by reducing the collector current to a value below that necessary to maintain the $\beta_1 \beta_2 = 1$ condition.

The functions of the two transistors are combined into a single PNPN diffused wafer The four drawings in Figure 2 are all equivalent representations for the CS

Firing Sensitivity

The CS is inherently a high sensitivity device This is because the input NPN transistor is designed to have high gain. It is therefore very useful for high gain switching directly from low level control signals Usually the CS eliminates the need for intermediate stages of amplification in control circuits

In those applications where the high sensitivity is not required, or not desired, any degree of reduced sensitivity can be achieved by gate biasing In fact some negative gate bias is recommended for all circuits to insure absolute "no fire" stability Since the CS has a very high gain, it should not be operated or tested with the gate open. Internal leakage current I_{AGO}, may be large enough to cause turn on, even at 25° C, if the gate is allowed to "float"

For many applications, stabilizing bias is easily achieved by a resistor between gate and cathode The resistance value is determined by the maximum operating temperature for the application. Since biasing reduces firing sensitivity, the correct resistance value is a key part of the circuit design.

Bulletin D420-01 covers the design considerations for bias stabilization in detail In less critical circuits where high gain is not the primary object, a 1K resistor will provide stabilization up to 125° C junction temperature A 1K resistor provides approximately 500 μA of bias current at 25° C The input firing current is therefore 500 μA plus the required gate firing current

A rapidly rising anode voltage resulting from switching transients or other sources, can couple a current into the gate through the anode to gate capacitance of the CS (approximately 25 $\mu\mu$f). This gate current can be sufficient to fire the CS The magnitude of the gate current is given by the expression. $i = C \frac{dv}{dt}$ where i is the instantaneous gate current, C is the anode to gate capacitance, and $\frac{dv}{dt}$ is the rate of rise of anode voltage Undesired firing due to the dv/dt effect can be eliminated by (1) sufficient negative gate bias current, (2) supply filtering, or, (3) a capacitor between anode and cathode A 01μf capacitor will usually be adequate

Input Characteristics

The input characteristics of the CS, gate to cathode, is similar to the base-emitter input of a conventional NPN silicon transistor Firing occurs at a specific value of input current and voltage

All CS s of a particular type will fire within a limited voltage range at a given temperature For one class of CS the firing voltage is specified at 52 ± 08V at 25° C Firing voltage is a predictable and uniform parameter Stabilizing bias is used to prevent gate voltage from floating up to the firing voltage level

Output Characteristics

Figure 1 shows the output E-I characteristic of the CS In the "off" condition, the CS will block both positive and negative voltages within ratings, applied between anode and cathode The output impedance of the device is extremely high, usually 10 megohms or more at 25° C When a positive gate signal is applied, the CS turns on and its impedance drops to a very low value The "on" impedance is below 1 ohm at an anode current of 1 amp. When "on" the characteristics of the CS closely approximate those of a conventional silicon diode or rectifier

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4 BASIC STATIC SWITCHING CIRCUITS

D C Source Voltage

With a D C voltage source, the CS acts as a latching switch Once turned on by a control signal, it will remain on indefinitely To turn it off, the anode current must be reduced to below the "dropout" level Figure 3 shows a simple latching switch circuit Resistor R_G provides a negative gate bias current and insures a stable "off" condition In this circuit, less than 20 microwatts input power (6V - 20 μA) for a time duration of 1 microsecond or longer will turn on load power up to 200 watts By proper choice of R_G, any degree of reduced sensitivity can be designed for

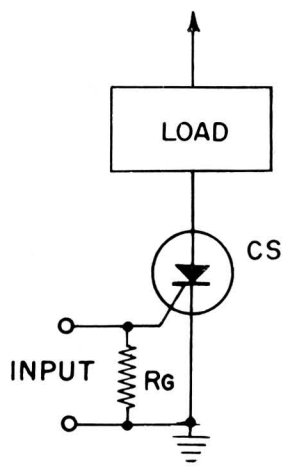

Fig 3 Simple latching switch.

The CS will latch on at any load current above the dropout level It will work as well with small loads (10 ma) as it does at higher load currents

The circuit in Figure 3 can be used as a single contact latching switch for direct control of a given load It is useful for driving relay coils or similar electromagnetic loads With the CS, a conventional D C relay can be converted to a high sensitivity latching relay For inductive loads a diode may be necessary across the load to eliminate voltage surge when the power is removed

For the simple latching circuit of Figure 3 turn off can be accomplished by removing the source voltage The CS can also be turned off by the arrangement shown in Figure 4 As before the CS is off until an input control signal turns it on When "on" the voltage at point A is approximately +1V Capacitor C charges through R_1 until point B reaches the full positive supply voltage When switch S is closed, point B is at ground and the

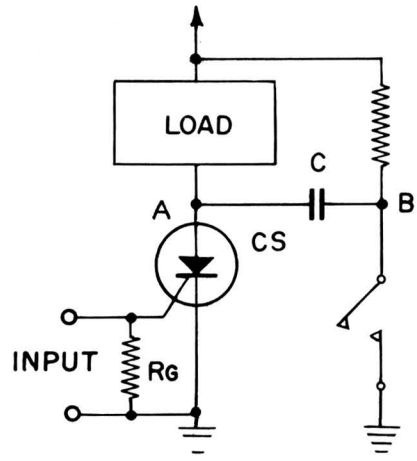

Fig 4 Shunt capacitor turn off

capacitor drives point A negative with respect to ground The current through the load is then diverted from the CS and begins to discharge the capacitor Since point A is negative, the CS will turn off This is called shunt capacitor turn-off The capacitor, C, must be sufficiently large to hold point A negative for the time required to turn off the CS The minimum value can be calculated from the relation: $C_{min} = \frac{25I}{E}$, where I is the load current in amperes and E is the supply voltage C_{min} is in μf This assumes a turn off time for the CS of 20 μseconds which applies over the temperature range of -55 to +100° C

If another CS is used in place of switch S, turn off can be accomplished electronically as shown in Figure 5 Operation is identical to that described above except that turn off is accomplished by a

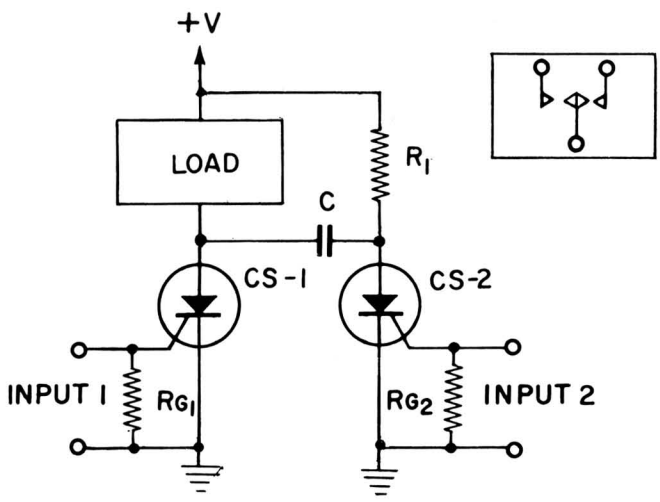

Fig 5 Power flip-flop or DPST static switch

mometary low level positive pulse at input 2 This circuit is actually a power flip-flop. When CS-1 is turned on, CS-2 is turned off by C When CS-2 is turned on, CS-1 is turned off by C A second load can take the place of R_1 so that DPST switching between two loads is easily accomplished This circuit is the static equivalent of the mechanical contact arrangement shown in the inset of Figure 5

Other turn off methods for D C circuits are described in SSPI Bulletin D420-01

A C Source Voltage

With an A C voltage source, the CS acts as a controlled half wave rectifier It will block both the positive and the negative half cycle until a positive control signal is applied to the gate When this occurs, the CS will conduct during the positive half cycle and block during the negative half cycle for as long as the control signal is present When the control signal is removed, the CS will block both half cycles again, since it automatically turns off at the end of each positive half cycle By proper timing of the applied control signal, the CS can be made to conduct for all, or part of, the positive half cycle Thus proportioning control of the output is possible, as well as on-off switching

Figure 6 shows a simple A C static switch which supplies rectified half wave D C to the load The

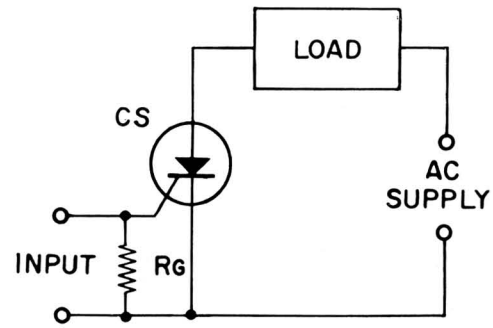

Fig 6 Half wave switch

input control signal can be A C , D C or pulse If the load is inductive a diode placed across it as shown in Figure 7 gives a continuous current through the load during the negative half cycle The inductive field built up during the positive half cycle returns stored energy during the nega-

tive half cycle The diode polarity is such as to allow this induced current to flow in the same direction as during the positive half cycle This technique is useful in driving loads such as relays or field windings where half wave pulsating current is undesirable

Figure 7 is a convenient arrangement for achieving low level control of D C relays in which latch on is not desired

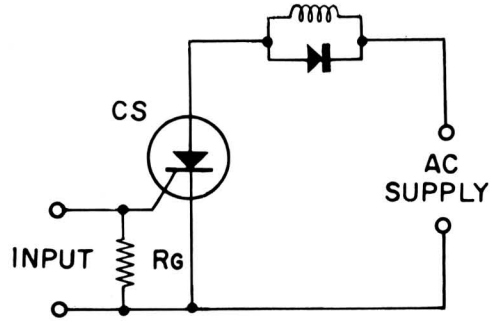

Fig 7 Half wave switch inductive load

In A C circuits, any positive control current applied to the gate during the negative half cycle must be limited to a low value This is necessary since transistor action in the CS will cause the reverse leakage current to increase in proportion to the positive gate current If this leakage current is too large, overheating and thermal runaway can occur The leakage current present during the reverse half cycle will be approximately 1/2 the value of the positive gate current A negative current which will cancel out any positive current that may be present during the negative half cycle is easily obtained by a diode and resistor as shown in Figure 8

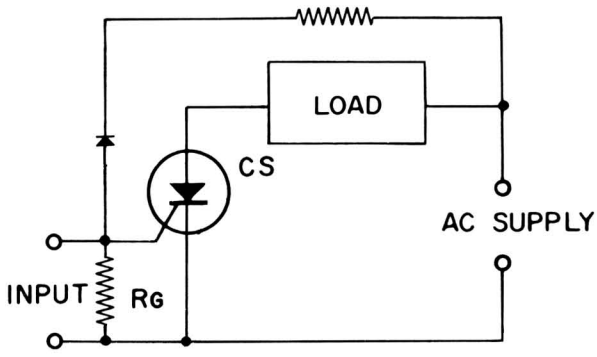

Fig 8 Negative gate biasing

A full wave D. C output static switch is shown in Figure 9 This is a conventional full wave bridge rectifier in which CS's are used in two legs In this circuit, an input control signal is supplied to CS-1 when its anode is positive This will turn CS-1 on for all or part of the half cycle During the next half cycle turn-on control signal is supplied to CS-2 when its anode is positive Proportioning control from zero to full output can be achieved by timing the control signals

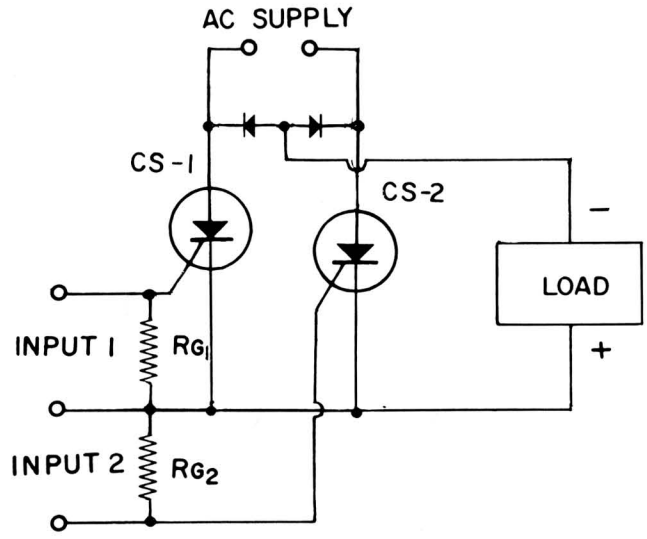

Fig 9 Full wave D.C output

A full wave A. C output switch is shown in Figure 10 The CS's work the same way as in the D C output circuit except that in Figure 10 the CS's are connected in inverse parallel for A C output

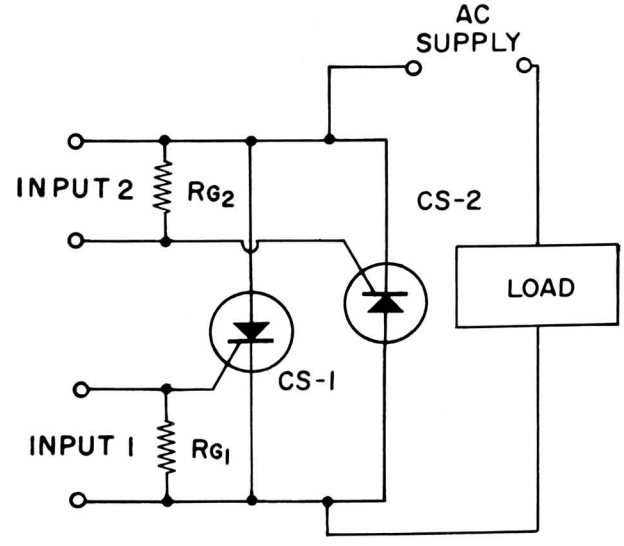

Fig 10 Full wave A.C output

and the two additional conventional rectifiers are not needed

In all of the static switching circuits discussed here, the CS is used to control the load power from a separate low level control signal input The load circuits are quite simple and straightforward Switching efficiency is high - up to 98%. When proportioning control is used to vary output from zero to full value, no power is wasted when the output is not at its full value Thus the CS acts as a "lossless electronic rheostat"

In the sections to follow, a wide variety of input control circuits are shown which permit many circuit functions to be easily and simply performed The time variable pulse generator (Section 11) is particularly suited for proportional control of the CS in A C circuits

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5 BASIC D C. PULSE AND SWEEP CIRCUITS

The CS can be used to generate high current - high voltage pulses using extremely simple circuitry Peak pulse currents as high as 20 amperes can be generated with voltage amplitudes up to 150 volts Output amplitude and wave shape are independent of the input pulse Input pulse amplitudes as low as 20 μA-0.6 volts will produce full output Thus extremely high power gain is possible Current gains up to 50,000 and voltage gains up to 200 can be achieved This represents a power gain of 10,000,000 Operating rep rates are limited by two factors, the maximum allowable power dissipation and the gate recovery time When power dissipation is not limiting, the CS can operate at rep rates up to 100 KC

Some of the applications in which CS pulse generators are useful include magnetic core switching radar and beacon modulators, clock generators, timing circuits, and time variable pulse generators for firing Silicon Controlled Rectifiers Both R-C and L-C pulse generator circuits can be used for generating sawtooth waveforms Since the CS has voltage ratings up to 200V in both the forward and reverse direction, high voltage outputs can be directly obtained.

R-C Pulse Generators

A triggered R-C pulse generator is shown in Figure 11 Capacitor C is charged to the supply voltage through charging resistor R_C When a trigger pulse is applied to the input, the CS fires, discharging C through load, R_L. This circuit can be triggered at any desired rep rate The output pulse amplitude will be a function of the rep rate, however, unless the time between pulses is greater than 3 $R_C C$ The output pulse voltage amplitude will equal the voltage across the capacitor less the drop across the CS The available output current is limited by R_L

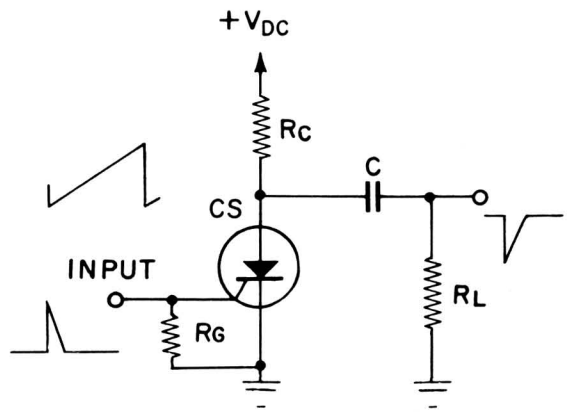

Fig 11

A modified version of this circuit is shown in Figure 12 In this case, the load resistance is placed in the cathode to obtain a positive output pulse Since this circuit behaves like an emitter follower, there are some special considerations When the CS fires, the voltage at its gate will rise to a value 0 5V above the voltage across R_L If this gate voltage is higher than the input trigger voltage the triggering circuit will act as a load drawing current from the gate A coupling diode can be used to eliminate this loading effect Since the CS turns on in approximately 1 μseconds, gate drive will be removed within this time if the input trigger voltage does not exceed the output voltage across R_L To insure that the CS will stay on when the triggering voltage is lower than the output voltage, the minimum gate driving current should be increased by a factor of 10 higher than the specified value This will provide the necessary energy into the gate during the first 0.1 μseconds to insure firing

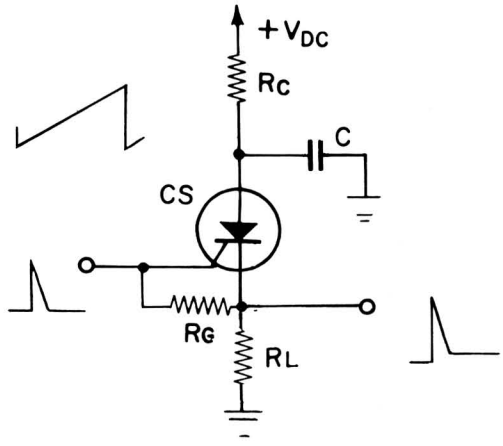

Fig 12

A third version of the R-C pulse generator is shown in Figure 13 This circuit is useful as a frequency divider in addition to pulse generation Frequency division to 1/10 is possible In this circuit the charging resistor, R_C, is in the cathode circuit and the load, R_L in the anode With no charge on the capacitor, the full supply voltage is across R_C This provides a large negative bias between gate and cathode Diode D_1 is in the reverse direction and prevents exceeding the gate to cathode voltage rating of the CS As the capacitor charges the voltage across R_C decreases toward zero The CS will fire when the voltage at point A decreases below the gate voltage by an amount equal to the gate firing voltage of the CS plus the forward drop of D_1 (approximately 1 volt total) Assume an input pulse amplitude of +2 5V between gate and ground an input pulse rep rate of 20 KC, and a supply voltage of 20V If the time for A to charge down to +1 5 volts is 500 μseconds then one output pulse will occur for each ten input pulses The output rep rate will be 2 KC and frequency division by ten has occurred

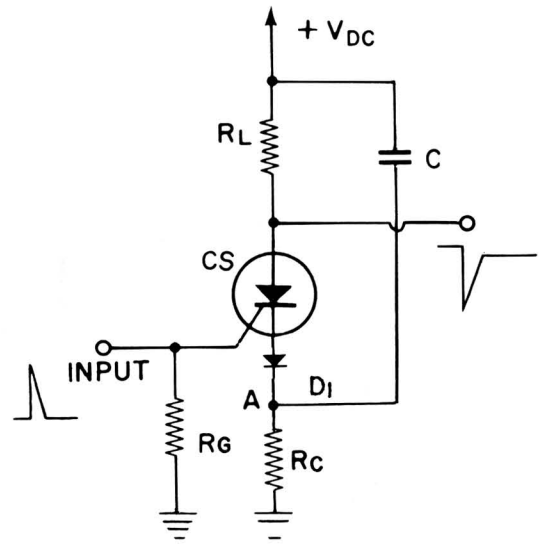

Fig 13

In R-C pulse circuits operating from a D C source and which require the CS to turn-off after each pulse output, R_C must be large enough to prevent the steady state current through the CS from exceeding the dropout value An upper limit also exists for R_C It must supply enough current to permit the CS to fire The requirement for a minimum value of R_C does not apply to circuits which are turned off by other methods For example the L-C pulse generators in the next section which turn off the CS by driving its anode negative

The R-C pulse generator circuits previously discussed are intended for use where a trigger input fires the CS They are not well suited for "free-running" or astable applications when the supply voltage is D C A "free-running" version of Figure 13 is shown in Figure 14 In this circuit a

square wave or similar source voltage is used to achieve turn-off of the CS One pulse output can be obtained for each half cycle of source voltage The time when the output pulse occurs will be directly related to the starting time of the source voltage, and the output pulse can be delayed with respect to the source voltage Resistor R_1 and R_G place a positive bias on the gate, with respect to ground This bias determines the time when the circuit will self trigger The circuit of Figure 14 is the basis for the time variable pulse generator discussed in Section 11

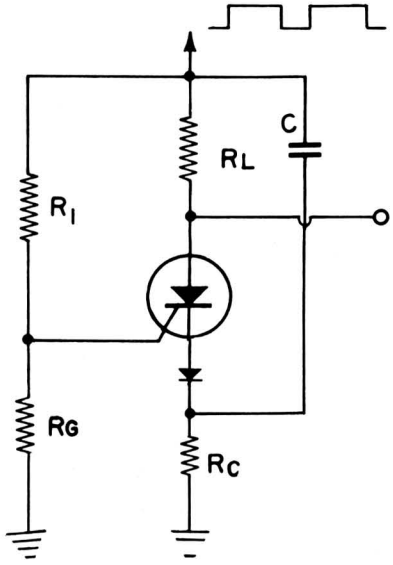

Fig 14

L-C Pulse Generators

L-C pulse generators have the advantage of higher operating rep rates than the R-C circuits previously discussed. The output waveform is a half sinusoid which is more useful in some applications The requirement for a minimum value of R_C, necessary for automatic turn off in the R-C circuits, does not apply to the L-C circuits since they accomplish turn off of the CS by taking the anode negative This permits greater design flexibility

A basic L-C pulse generator is shown in Figure 15 The capacitor C charges through R_C to the supply voltage When an input trigger pulse turns on the CS, the capacitor resonantly discharges through L, R_L, and the CS This gives a negative half sinusoid of current through R_L with a pulse width at the base determined by the resonant frequency of the loop. When the current through the loop goes to zero, the voltage across the CS goes negative, turning it off A small positive output will occur due to the recovery current flowing through the CS A diode across R_L will limit the amplitude of this positive to +0.5V if desired. The L-C pulse generator depends on "ringing" of the resonant loop to turn off the CS at the end of the first half cycle by driving the anode negative The resonant circuit must therefore be underdamped with R_L less than X_L at the resonant frequency

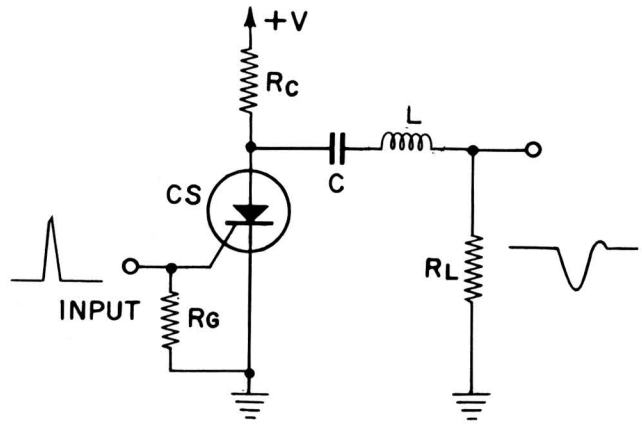

Fig 15

Since the CS limits the resonant discharge to a half cycle, the capacitor ends up charged to approximately the supply voltage value, but in the negative direction. Therefore, after the output pulse is over, the capacitor will begin charging toward +V from -V The recharging time constant will be determined by R_c and C Resonant recharging can be employed if R_c is replaced with an inductance and a charging diode is added In this case C charges to approximately twice the supply voltage if the circuit Q is high. The series resistance of L_1 should be large enough to limit the current through the CS to below its average rated value This will prevent damaging the CS if, for any reason, it gets turned on continuously Figure 16 shows a resonant recharging circuit

In the L-C pulse circuits it is important that the anode of the CS remain negative for a time exceeding the gate recovery time If this is not observed, the CS will turn on by itself as soon as

the anode voltage goes positive during recharge This limits the upper operating rep rate but places no restriction on the output pulse width or peak current

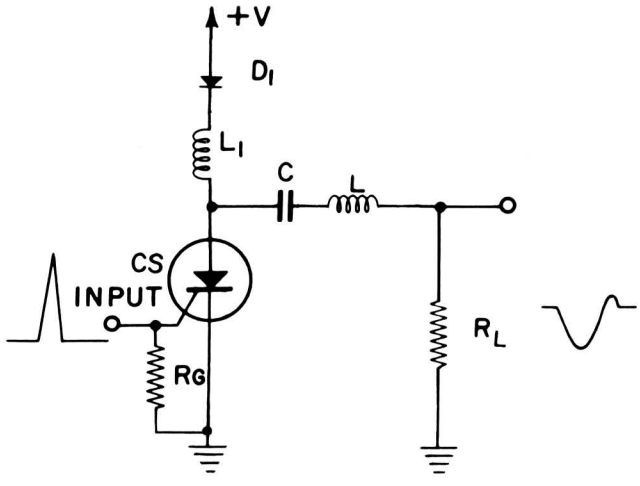

Fig 16

Figure 17 shows another version of the L-C pulse generator which provides a positive output pulse

In either the R-C or the L-C pulse circuits, using

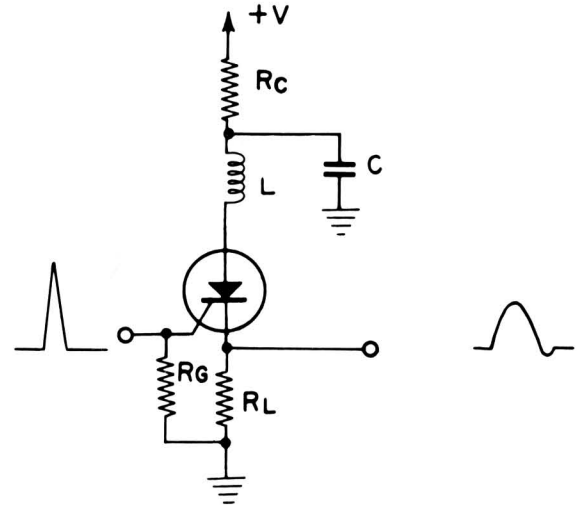

Fig 17

a transistor in place of R_C will give constant current charging and therefore a linear rather than an exponential charging rate The L-C circuits are readily adaptable to "free running" or astable applications A zener diode connected between anode and gate will provide the necessary feedback and set the firing point

6 VOLTAGE LIMIT DETECTORS

The properties of the CS make it particularly useful in voltage limit detectors and related voltage or current threshold actuating circuits The high sensitivity series with maximum gate firing current of 20 μa, and 0.52 ±0 08V gate firing voltage, have been specifically u signed for this type of application. The threshold firing point can be set at any desired value from 0 60V up by the use of an input voltage divider or zener diodes

The voltage limit detectors can use either D C or A C load power If D C is used, the C S will "latch on" when the input exceeds.the threshold voltage If A C load power is used, the CS will supply power to the load only when the input voltage exceeds the threshold voltage

Voltage limit detectors, using the C_S, are quite simple and useful in a variety of timing, sensing, indicator warning and safety applications Since the CS can handle high load power, it can directly actuate the controlled circuit in many cases A low power input from pressure temperature speed, flow, light, or similar transducers can be made to turn on the CS at a preset level The CS can then actuate a control circuit, relay, solenoid buzzer indicator light, horn or similar output

The simplest form of a voltage limit detector is

shown in Figure 18 This circuit takes advantage of the fact that the CS will not turn on until the minimum gate firing voltage has been exceeded at point A The ratio between R_1 and R_G determines the threshold firing voltage at the input The firing voltage of the CS has a negative temperature coefficient of approximately 3 millivolts per degree C If a uniform firing voltage at the input is desired over a wide operating temperature range, compensation will be necessary

The value of R_G is determined by the required bias off current at the upper operating temperature to insure a stable "off" condition for the CS

Where operation will be at temperatures above 100° C the basic circuit of Figure 19 may be preferred With a negative bias supply, R_G can be larger than when it is returned directly to the cathode Larger R_G will also reduce current loading on the input

A zener diode can be used to set the input threshold, as shown in Figure 20, where a higher input voltage and minimum loading is desired A zener diode with a positive temperature coefficient can be used to compensate the negative coefficient of the CS A further degree of refinement could be achieved by using a negative temperature coefficient resistance for R_G to compensate for changes in firing current with temperature Thermistors will provide a negative coefficient of resistance

Another arrangement which uses positive cathode bias is shown in Figure 21 A diode, D_1, is neces-

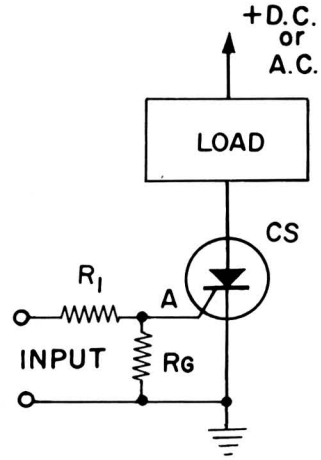

Fig 18

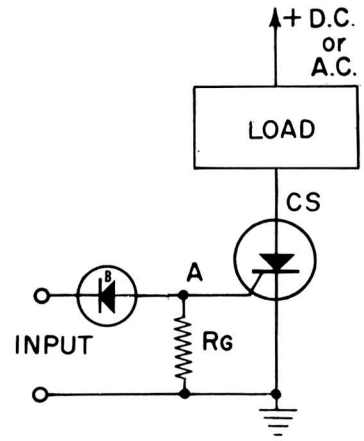

Fig 20

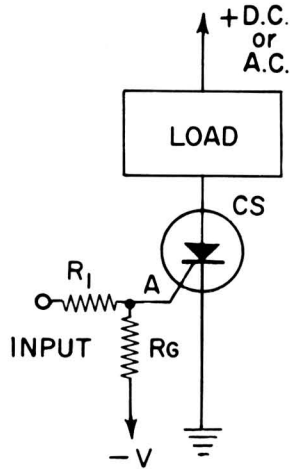

Fig 19

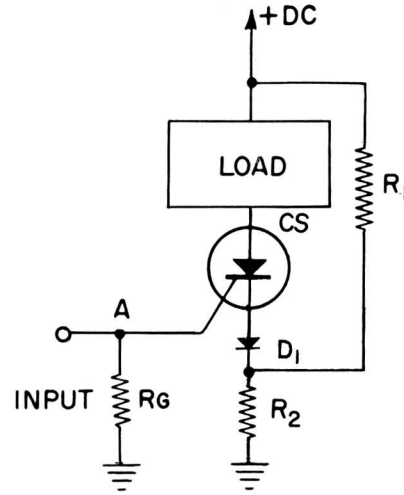

Fig 21

sary if the voltage across R_2 exceeds +5 volts In this circuit the threshold is a fixed proportion of the supply voltage This is useful if a changing threshold, as a function of changing supply voltage, is desired R_2 could be replaced by a zener diode if a fixed or temperature compensated threshold is desired With a zener diode in the cathode circuit, R_1 and D_1 can be eliminated This circuit provides excellent bias stabilization for the CS and permits operation up to 150° C

In each of these circuits, the CS will fire when the voltage at point A, with respect to the cathode, is at the specified firing voltage for the CS; and the current required at point A is equal to the minimum gate firing current plus the current required through RG to develop the necessary firing voltage

---

7 TIMING AND TIME DELAY CIRCUITS

The voltage limit detectors discussed in the previous section are readily adaptable to R-C timing and time delay circuits As a voltage limit detector, the CS will turn on after a preset threshold voltage at the input has been exceeded This input voltage can be obtained from a capacitor being charged at a specified rate Thus a fixed time delay can be established by controlling the rate of charge on the input capacitor and the threshold point This type of circuit will act as a time delay static switch. Delay times up to 20 seconds are possible and the circuits can be put in series for longer times A time delay static switch of this type can be made very small in size yet control more than 100 watts of load power Timing accuracy of better than ±5% can be achieved under varying temperature and supply voltage when the circuits have been properly compensated

A time delay static switch using a zener diode to establish the voltage threshold is shown in Figure 22 This circuit is the basic voltage limit detector shown in Figure 20 with the addition of a timing capacitor and resistor Figure 23 graphically shows the relation between firing time and the input voltage Curve 1 is the charging rate during the period when the voltage across C is less than the zener diode voltage, V_{Z1} This is established by the value of C, R_C, R_L, the leakage current of C and the leakage current of the zener diode

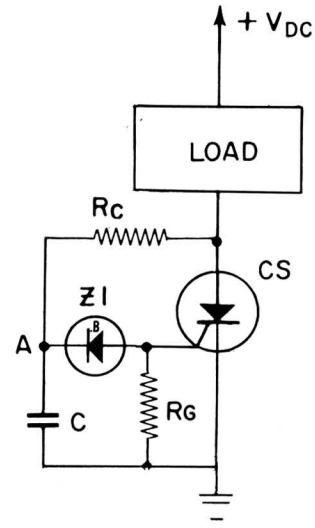

Fig 22 Time delay static switch.

When the voltage at point A equals the zener diode voltage current will begin to flow from R_C through the zener diode into R_G and into the gate of the CS This occurs at time t_1 on the curve The additional current through the zener diode reduces the capacitor charging rate and the voltage build up on C will now follow Curve 2 The voltage at A must rise by an additional amount equal to the firing voltage of the CS V_{GCF}

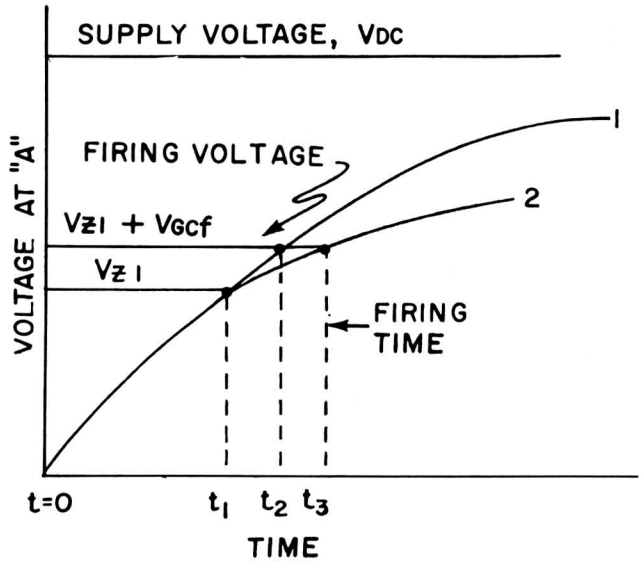

Fig 23

If no additional loading were present on C when it passed the V_{Z1} voltage, it would continue charging along Curve 1 and the CS would fire at time t_2 Since there are loading effects present, however, the actual firing time is t_3

Since R_C must supply both the charging current for C and the gate firing current, it has a maximum value based on the minimum current it must supply This minimum current is the sum of the charging current, the capacitor leakage current, and the current into the zener diode for firing. The current into the zener diode is: $I_{Z1} = I_{Gf} + \frac{V_{GCf}}{R_G}$, where I_{Gf} is the maximum firing current for the CS and V_{GCf} is the maximum firing voltage of the CS

The maximum value of R_C is given by the expression: $R_C = \frac{V_{DC} - (V_{DZ1} + V_{GCf})}{I_{min}}$; where V_{DC} is the supply voltage, V_{DZ1} is the zener diode voltage, and V_{GCf} is the maximum firing voltage of the CS I_{min} is determined from the sum of the currents mentioned in the preceding paragraph. This expression assumes R_L is much smaller than R_C

In the circuit of Figure 22, the time delay will be a function of the supply voltage since this determines the charging rate To make the time delay independent of supply voltage variations, a second zener diode and resistor can be added, as shown in Figure 24, to give a constant charging voltage for C

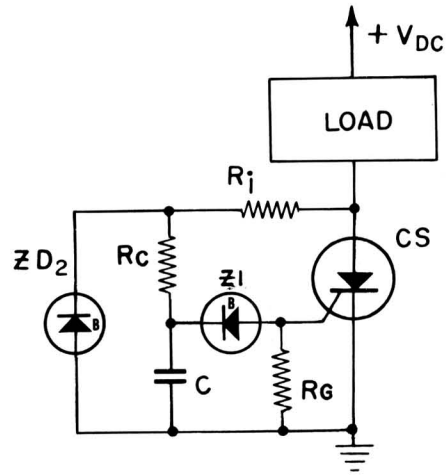

Fig 24

The circuits of Figure 22 and Figure 24 are relatively immune to premature firing due to line voltage transients A small capacitor (approximately 01 μf), directly across the CS from anode to cathode, may be necessary if the line transient is fast This capacitor will prevent the transient from being coupled to the CS gate by internal anode to gate capacitance

The timing circuits discussed previously commence their timing cycle when the supply voltage is applied In some applications it is desirable to start the timing cycle from an electronic pulse at any point in time after the supply voltage is applied This can be accomplished by adding a CS and two resistors as shown in Figure 25 In this circuit, the timing capacitor will remain uncharged until CS-2 is turned on, clamping point A to approximately +1 volt When CS-2 is turned on, C commences charging and will fire CS-1 after the preset time delay Load current will flow through both CS-1 and CS-2 The current through R_1 need only be large enough to exceed the dropout current of CS-2 Two or more timing circuits can be connected in series to achieve longer time delays by this same technique

An interval timer, or high power one-shot multivibrator can be made by combining the time delay static switch of Figure 22 with the power flip-flop of Figure 5 Such a circuit is shown in Figure 26.

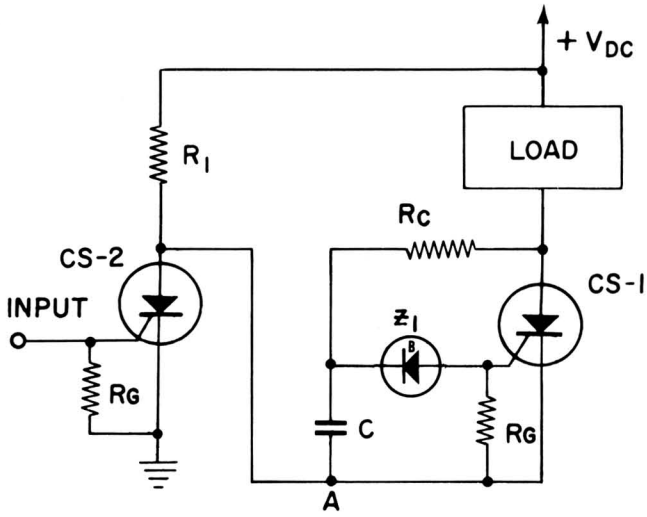

Fig 25

When supply voltage is applied, CS-1 will turn-on after the preset time has elapsed An input pulse will turn on CS-2 This turns off CS-1 by the action of the commutating capacitor, C1 When CS-1 has been turned off, C will commence charging and will turn on CS-1 after the preset time interval This turns off CS-2 by the action of the commutating capacitor and removes load power An input pulse should not be applied to CS-2 for a time period equal to 2 to 3 times the delay time after the supply voltage is first turned on. The time interval between input pulses should also equal at least 2-3 times the delay time This is necessary to permit C to discharge after CS-2 has turned on, and to allow C_1 to fully charge to the correct polarity

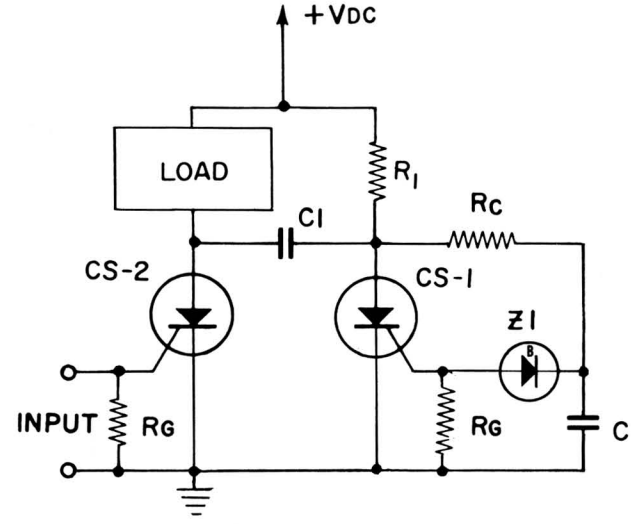

Fig 26 Interval timer (one shot multivibrator)

8 PROTECTIVE CIRCUITS

Nearly all electronic circuitry requires some means of protection against excessive voltage transients, overloads and similar unexpected trouble The problem of protecting transistor circuits is particularly important since transistors can be easily damaged by excessive voltage Mechanical circuit breakers and fuses are usually not too useful because they respond too slowly are too big, or cannot be easily reset In addition, these devices are primarily current actuated and offer little protection against voltage overload.

The CS or SCR can be used to give excellent protection to many types of systems Figure 27 shows a simple arrangement that will protect against excessive supply voltage The CS will turn on when the voltage at A exceeds approximately 6 volts With the voltage divider values used, this would occur when the input reached +35V When the CS turns on, the voltage to the load will drop to approximately +2V The current through the CS is limited to safe value by the 27 ohm resistor This circuit will respond within .2 μseconds after the overvoltage occurs The

response can be slowed down to any desired degree by a capacitor across the 1K resistor The circuit can be manually reset by turning off the supply voltage momentarily If electronic reset is desired, a second CS in the power flip-flop connection can be used This is shown in Figure 28 A positive pulse at the reset input will turn off CS-1 and restore voltage to the load

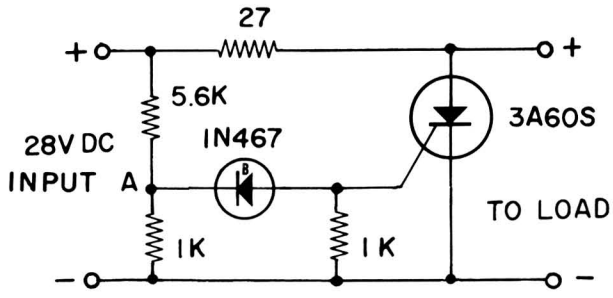

Fig 27 Overvoltage protection

An equally simple arrangement can be achieved for overcurrent protection. Figure 29 shows a circuit which can be turned on and off electronically and will turn itself off when the load current exceeds a pre-set maximum value Manual turn-on and turn-off is also provided This again is the basic power flip-flop. Load power is turned on by turning on CS-2 This can be accomplished either by a positive pulse input at the "on" lead or by depressing the "on" switch momentarily The circuit will remain on unless the load current, passing through the 4 7 ohm resistor, rises to a point where the voltage across this resistor exceeds the critical threshold voltage set by the zener diode and turns on CS-1 When this occurs CS-2 is turned off by the commutating capacitor and the load circuit is opened The load power can also be removed by a positive pulse at the "off" lead or by depressing the "off" switch momentarily With values shown, the trip point is approximately one amp

Overvoltage and overcurrent protection can be combined to protect a single load by combining the circuits of Figures 27 and 29 It can be designed so that if overvoltage occurs, the current drawn by the voltage protecting CS actuates the overcurrent portion of the circuit and therefore opens the load circuit This automatically resets the voltage protecting part of the circuit An electronic reset pulse or manual turn on switch can then re-apply load power

The design of protective circuits using the CS or SCR is very flexible Circuits requiring voltage up to 200 volts - 1.25 amps can be protected The tripping current level can be set as low as 20 mA

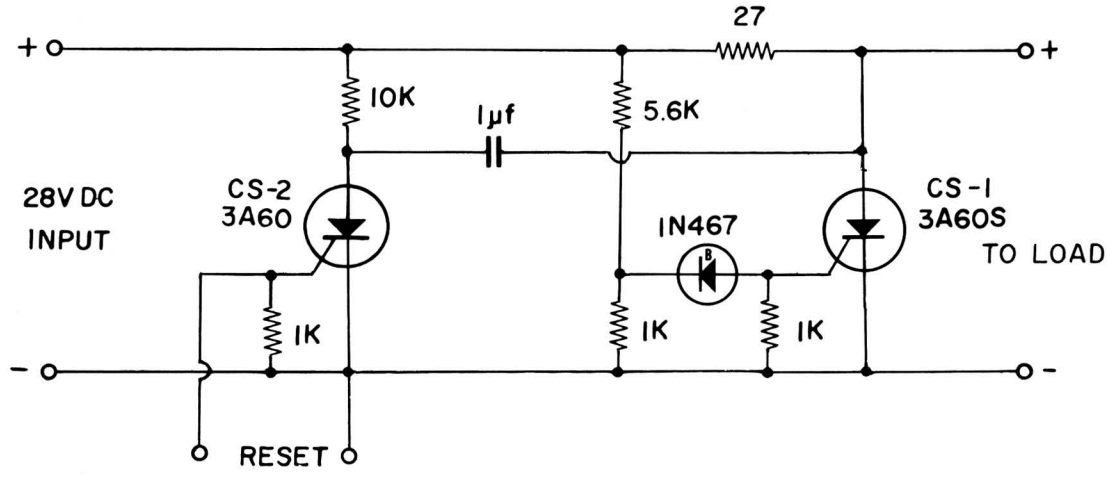

Fig 28 Overvoltage protection electronic reset

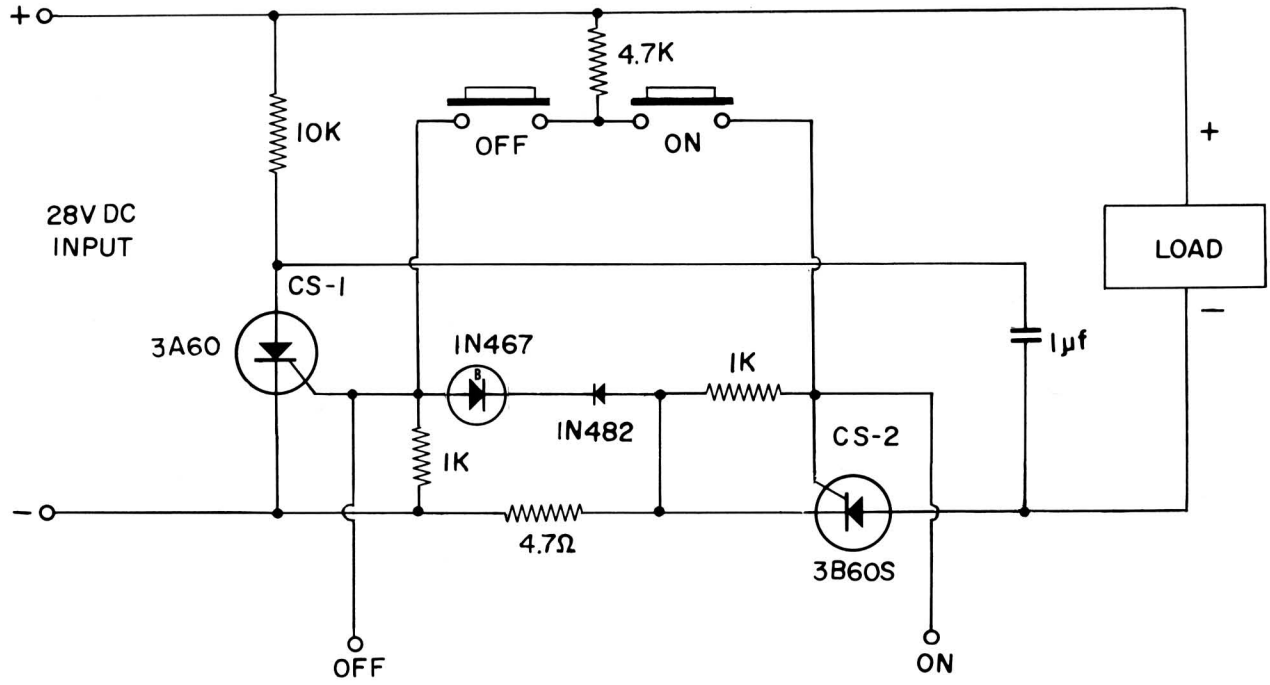

Fig 29 Overcurrent protection.

9 LOGIC INPUT CIRCUITS

A variety of logic input circuits are possible with the CS In fact most of the logic inputs that are used with transistors can be adapted for use As with many previous CS circuits, either A C or D C load power can be used The logic inputs are useful in data processing, control, indicator, protection, and fusing applications

Three simple "and" circuits are shown in Figures 30, 31 and 32 In each case, the circuits can be designed so that the CS will turn on only when there are inputs at both A and B In Figure 30 one of the inputs is the anode source voltage while the other is the gate signal In Figure 31, the gate is negative biased The input signals are positive and must be limited in amplitude so that with either input present, the gate remains negative biased but with both present, the gate to ground voltage exceeds the firing requirement and the CS turns on In Figure 32, the CS is normally biased off by a positive cathode voltage In this case the inputs must be negative When both inputs are present, the positive bias is overcome and the cathode goes negative by an amount exceeding the firing requirements of the CS

Figures 31 and 32 can be used as "or" circuits by increasing the amplitude of the input signals so that either one will turn on the CS Figure 33 shows another version of an "or" circuit In this case either a positive input at A or negative input at B will turn on the CS

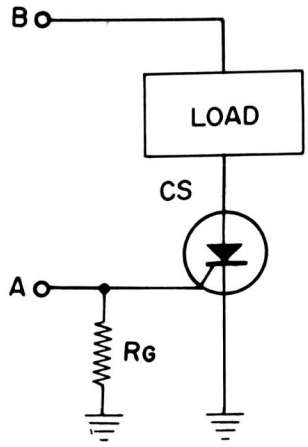

Fig 30 Simple "AND"

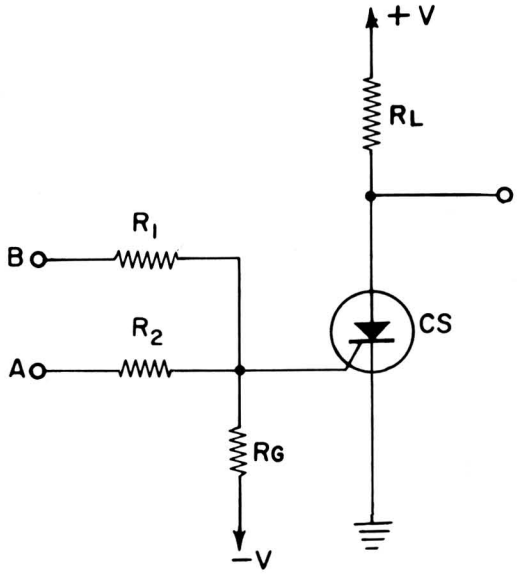

Fig 31 Positive input "AND" or "OR"

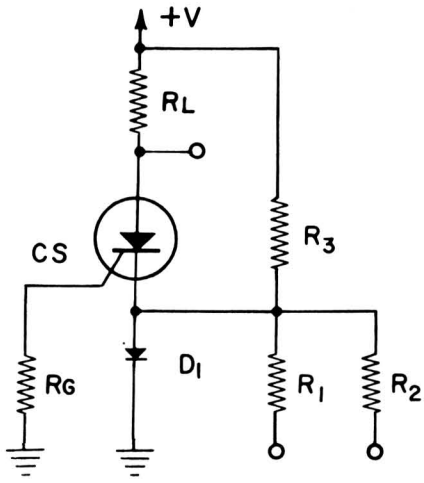

Fig 32 Negative input "AND" or "OR"

By combining the inputs shown in Figure 31 and Figure 32 a single circuit with four inputs is achieved A variety of "and" plus "or" combination can then be established Additional inputs can be added to such a combination as long as biasing is properly set

Figure 34 shows a sequential "and" circuit which is useful for safety, protective, fusing, and related applications Before power can be applied to R_L, three pulse inputs must be applied in the correct sequence

With all three of the CS's off, the bias voltage at input B is 1/3 of the supply voltage, and at input C it is 2/3 of the supply voltage CS-2 will not turn on unless the voltage applied at point B exceeds 1/3 of the supply voltage Similarly, CS-3 will not turn on unless the voltage at C exceeds 2/3 of the supply voltage CS-1 on the other hand will turn on with an input at A equal to the normal CS firing requirements Thus if the input pulse amplitudes are limited to less than 1/3 of the supply voltage, CS-2 cannot turn on until CS-1 has first been turned on Also CS-3 cannot turn on until both CS-1 and CS-2 have been turned on

A pulse counter circuit is shown in Figure 35 CS-1 and CS-2 are used as memory elements CS-3 turns on the load power after three positive input pulses have been applied at the input The first positive input signal at A couples through C_1, to turn CS-1 on Diodes D_2 and

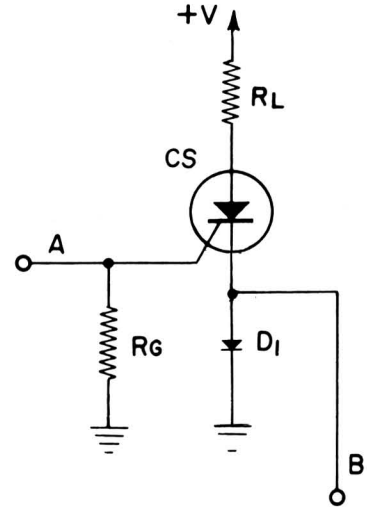

Fig 33 "OR" circuit

D_3 are biased in the reverse direction by the charge on C_2 and C_3, and block the input pulse from the gates of CS-2 and CS-3 After CS-1 turns on, the voltage at its anode is approximately +1 volt and C_2 discharges When the next positive input pulse occurs, it can now couple through D_2 to turn on CS-2 Again D_3 blocks this pulse from the gate of CS-3 When CS-2 turns on, its anode voltage drops to +1 volt and C_3 discharges The third positive input pulse can now couple through D_3 to turn on CS-3 and apply power to the load R_1 and R_2 must provide current above the dropout level to CS-1 and CS-2 The circuit can be made to reset electronically by adding another CS, in the power flip-flop connection as shown in Figure 35A.

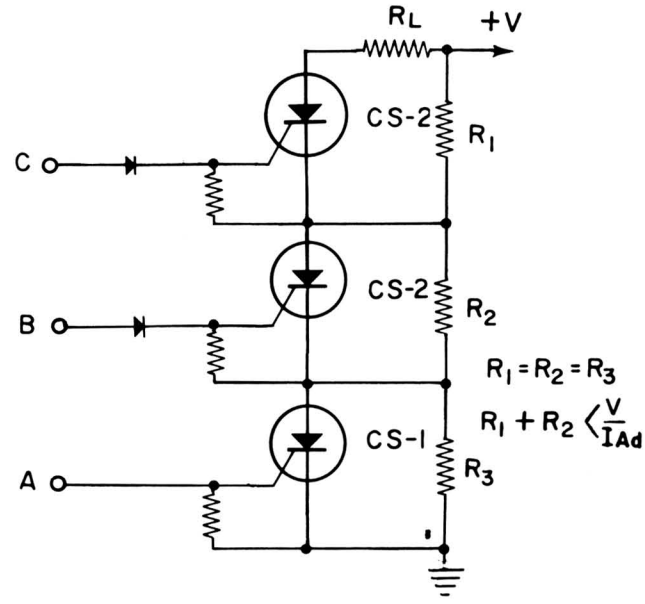

Fig 34 Sequential "AND"

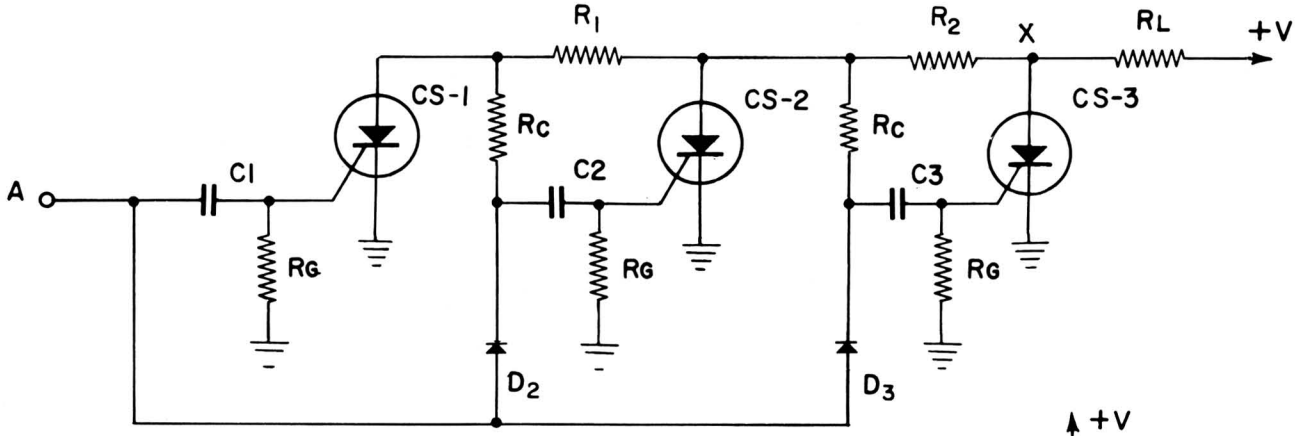

Fig 35 Pulse adder

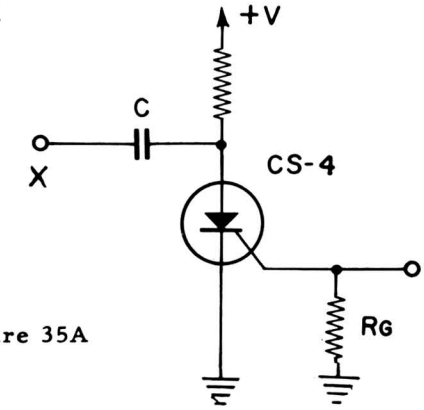

Figure 35A

10 SQUIB FIRING, FUSING, AND DETONATING SYSTEMS

The high surge current and peak power handling capabilities of the CS and SCR make them particularly useful in detonating applications For short time durations, the CS can supply high peak power Up to 2000 watts (100V-20A) can be supplied to a load for 10 μseconds This is 200,000 ergs of firing energy Considerably greater energy can be delivered to the load with lower current - longer time conditions The CS can supply 5 amps for 50 milliseconds which, with a 28 VDC source, amounts to approximately 6,000,000 ergs of firing energy Many test cycles can be made without damage to the CS Their small size permits a high degree of miniaturization.

Simple R_C time delay, as shown in Figure 22, can be easily introduced to the firing circuit The sequential "and" circuit in Figure 24, as well as other logic inputs can be used with any desired degree of redundant design to provide the desired safety features Absolute "no fire stability" for the CS can be established based on the minimum gate firing voltage Almost any degree of CS firing sensitivity can be achieved by proper circuit design.

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11 TIME VARIABLE PULSE GENERATOR FOR FIRING SILICON CONTROLLED RECTIFIERS AND SWITCHES

The preferred method of firing Controlled Rectifiers is by a high energy short duration pulse The best timing accuracy is achieved with a pulse having a fast rise time (0 5 μsec or less) It is not necessary, and in some cases undesirable, to have a continuous gate signal present When the SCR is conducting in the forward direction, continuous gate signal simply increases device dissipation without contributing to performance When the SCR anode voltage is negative, a positive gate signal substantially increases leakage current and therefore device dissipation Pulse firing avoids these two undesired conditions

A time variable pulse generator, which has been specifically designed for firing high power as well as low power SCR s is shown in Figure 36 This circuit is an adaptation of the pulse generator shown in Figure 14 The pulse generator will deliver 5V-200 ma pulses with a pulse width of 6 μsec or longer Pulse transformer output is used to provide isolation between the SCR s being triggered As shown, it is designed for 60 cycle operation Control is achieved from approximately 10° to 180° of the AC half cycle The

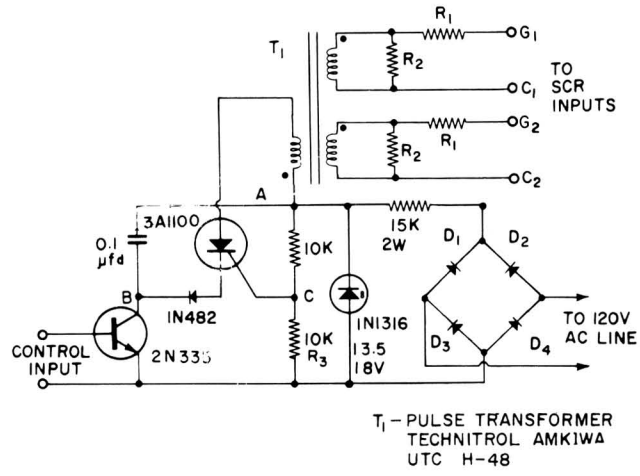

Fig 36 Time variable control circuit for firing SCR

circuit consumes very little power and a subminiature zener diode can be used The 15K current limiting resistor has the highest dissipation; approximately 0 7 watts at 120 VAC A 2N335 silicon transistor controls charging current to the 0.1 μfd capacitor and provides electronic control of the time delay Since the transistor is a constant current device, the charging rate is linear rather than exponential Thus, the time delay for firing is inversely proportional to the controlling input current at the base of the 2N335 transistor A variable resistor can be used in place of the transistor if manual control is desired

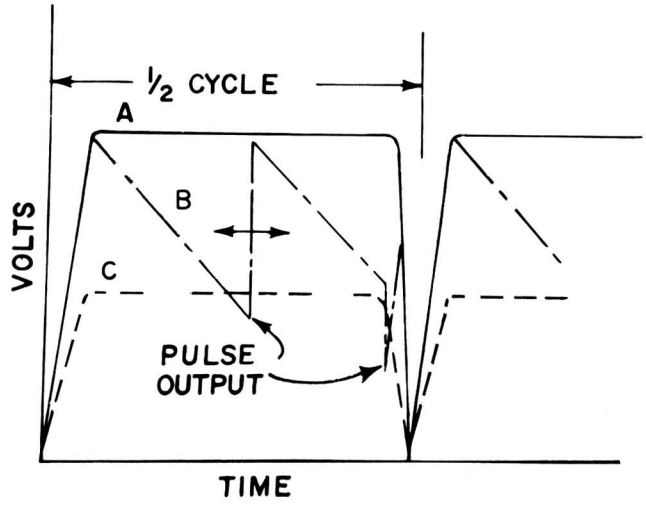

Fig 37

The circuit operation is quite straightforward The AC line voltage is bridge rectified by D_1 through D_4 so that pulsating D C is obtained at point A D_3 and D_4 are not required if the AC supply voltage is center-tapped The zener diode and the 15K resistor limit the voltage at A as shown by the waveform of Figure 37 A resistor divider consisting of two 10K resistors, supplies a bias voltage to the gate of the 3A16 equal to half of the zener voltage At the beginning of each half cycle the capacitor is discharged and the voltage at point B is equal to the zener voltage Thus the cathode of the 3A16 is positive with respect to its gate and the CS is biased off The 1N482 diode is also reverse biased to minimize loading effects on the timing capacitor and to prevent exceeding the cathode-gate voltage rating of the 3A16 As collector current of the transistor charges the capacitor, the voltage at point B drops toward zero. When this voltage drops below the fixed bias on the gate by an amount sufficient to fire the 3A16, the CS will turn on, discharging the capacitor into the primary of the pulse transformer

If for any reason, the capacitor does not charge sufficiently to fire the CS before the end of the half cycle, the CS will fire when the voltage at point A drops toward zero at the end of the half cycle When the voltage at A drops to zero, the gate bias voltage for the 3A16 is also zero However, with the capacitor partially charged, the voltage at B goes negative, causing the CS to fire and discharging the capacitor Timing for the next half cycle therefore starts with the capacitor discharged

Where possible, it is desirable to obtain the AC voltage for the control circuit directly across the SCR's being controlled This removes the supply voltage to the control circuit after the SCR fires, and eliminates unnecessary dissipation in the control circuit

The impedance reflected into the primary of the pulse transformer should be low (20 to 50 ohm) and primarily resistive Termination of the secondary windings as shown in Figure 36 is desirable The input impedance of the rectifier being controlled will affect the termination For low power units such as the SSPI 3A or 3B series, R_1 and R_2 should be 100 ohms High power units such as the C35 which require relatively high firing current can be driven directly from the secondary windings Series resistance of the pulse transformer secondary windings will provide the necessary decoupling without the need for R_1 and R_2 The 0 1 μfd capacitor should be replaced by 0.2 μfd to furnish the higher energy requirements of the high power SCR s

The circuit of Figure 38 is the same as Figure 36 except that the single control transistor is replaced by a pair of 2N335 transistors connected as a balanced input amplifier R_3 in Figure 36

is replaced by a voltage divider, R_4 and R_5, which provides a reference of 5 volts to the base of Q_2

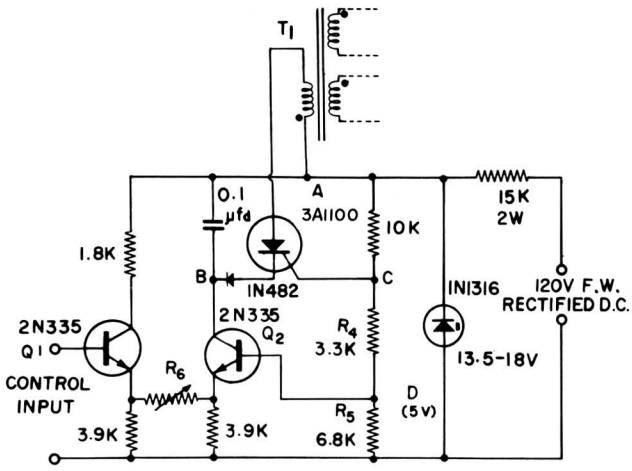

Fig 38 Control circuit with balanced input amplifier

The balanced amplifier is self-compensating for temperature variations of transistor parameters Its flexibility makes it attractive for a wide variety of control applications

The two 3 9K resistors in series with the emitters of Q_1 and Q_2 act as constant current sources, establishing the total emitter current of both transistors at approximately 2 mA. With a control input voltage of 5 volts applied to the base of Q_1 (the same as the reference voltage applied to Q_2) the two transistors share equally the 2 ma total available emitter current Q_2 therefore provides a charging current of 1 mA to the 0 1 μfd capacitor. Under this condition, R_6 has no effect on the circuit, since the current through it is zero.

When the control input voltage is raised above 5 volts, Q_1 demands more current, taking it from Q_2 through resistor R_6 When the control voltage is below 5 volts, current through Q_1 is reduced and charging current through Q_2 increases The center of the proportioning control voltage range is established by the reference voltage applied to the base of Q_2 A zener diode or any other voltage reference may be used in place of the simple voltage divider if greater reference stability is desired

Resistor R_6 controls the gain of the balanced amplifier and can be used to adjust the proportioning control voltage range above and below the 5 volt center When R_6 is zero ohms, gain is maximum Pulse delay is approximately 10° (almost full output) when the control input voltage is 4 9 volts, and 170° (almost no output) at 5 1 volts input Thus, a 4% input voltage change can control the SCR's from essentially zero to full power output Increasing R_6 reduces gain and broadens the proportioning range without altering the range center

In the control circuit as shown in Figure 38, an increase in control voltage causes a decrease in power output, and vice-versa By applying the reference voltage to the base of Q_1 and the control input to the base of Q_2, the control sense can be reversed if desired

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12 PROPORTIONING CONTROL CIRCUITS

When used with AC load power, the CS or SCR will block during both half cycles unless a gate signal is supplied The CS or SCR can be turned on at any point during the positive half cycle as long as the anode is more than 3 volts positive with respect to its cathode By properly timing a gate signal, the output of the CS or SCR can be made continuously variable from no output to full output Figure 39 shows the output voltage or current as a function of firing angle for a full

wave D C output with resistive load Since the internal dissipation of the CS or SCR is very low, nearly lossless proportioning power control can be achieved The low power requirements for gate firing permit the design of simple very high gain proportional control amplifiers

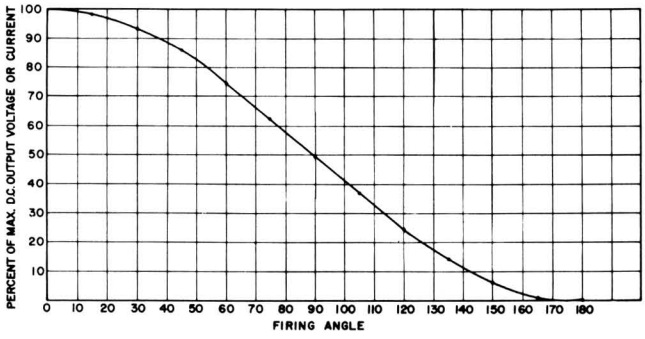


Fig 39 D.C output voltage vs firing angle

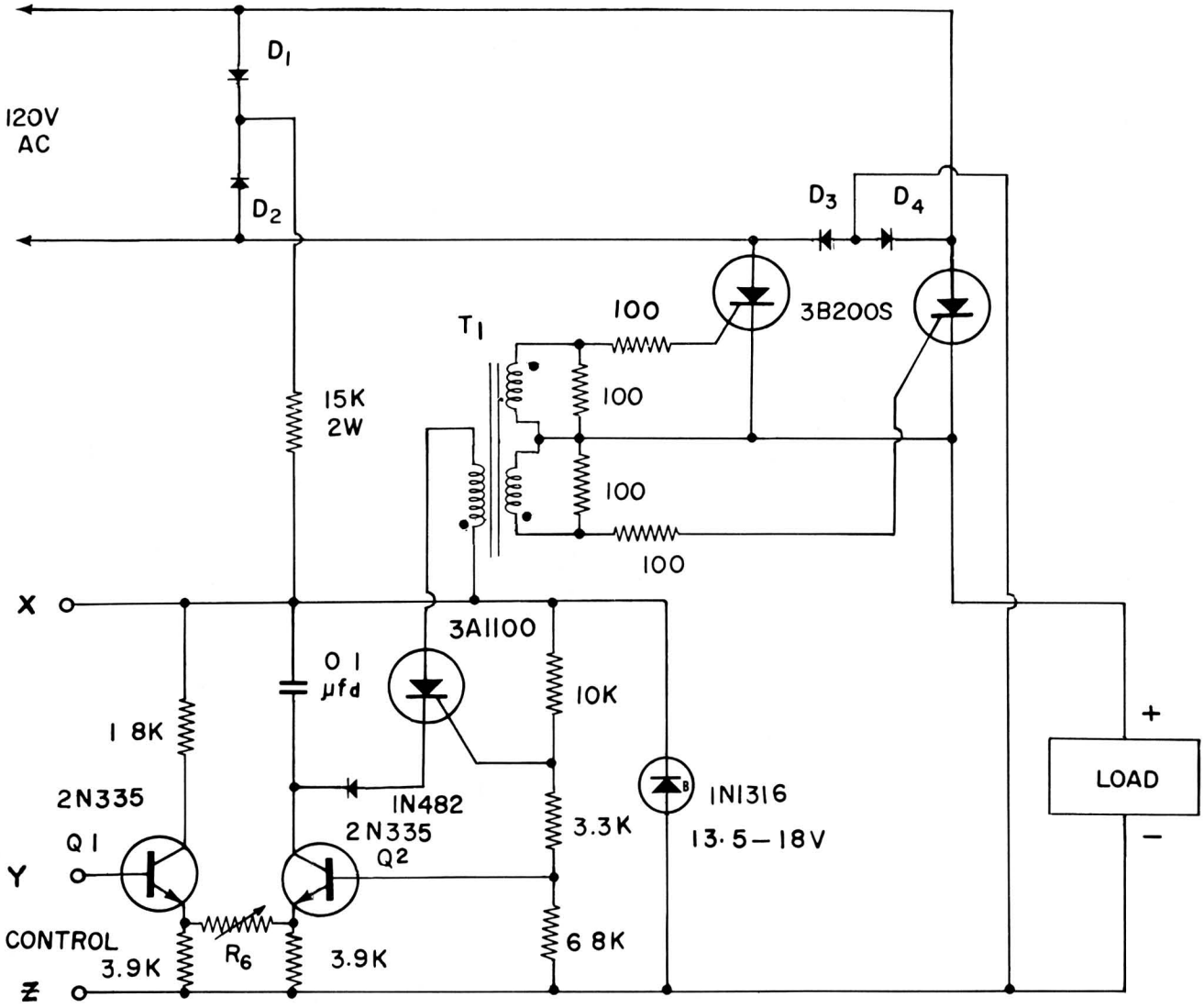
The time variable pulse generator of Figure 36 or 38 offers one means for achieving the desired gate signal control for proportional control systems This circuit will provide an output pulse variable from approximately 10^{o} to 180^{o} as a function of its input current By using this or similar gate control circuits, in conjunction with the basic full wave DC and AC circuits shown in Figures 9 and 10, proportional control is quite simply accomplished

Figure 40 shows a proportioning control amplifier with full wave rectified D. C output, incorporating the control circuit of Figure 38 A D C input voltage variable from 4 9 to 5 1 volts will provide full output control This circuit is useful for servo motor driving, temperature control and related applications Closed loop feedback is easily achieved for self regulating systems Full wave AC output can be obtained by using the output circuit shown in Figure 10.

The power control circuit of Figure 40 becomes a regulated D C power supply by applying part of the D C output voltage to control input Y Since the control reference is approximately 5 volts, a voltage divider across the load will regulate the D. C output voltage to 5 volts multiplied by the divider ratio. If the load voltage is unfiltered, it may be desirable to place a small capacitor across the control input

Regulated D C power supplies using the SCR eliminate the need for high dissipation series control elements such as power transistors or tubes This greatly minimizes heat sink requirements and permits smaller packaging In addition, they provide a wide control range A possible disadvantage is their response time, which can be no faster than the time of one half cycle of the supply voltage

By connecting a resistor from X to Y and from Y to Z in the control circuit of Figure 40, a bridge circuit is formed together with the resistor network connected to the base of Q_2 This forms the basis for many simple and reliable power control circuits, by using a variable resistance transducer as one of the two resistance elements at the input Examples include resistance thermometers for temperature control application and photoconductive cells for light control



D_1, D_2 – 200V SILICON DIODES
D_3, D_4 – 200V SILICON RECTIFIERS
T_1 – TECHNITROL AMK1WA

OUTPUT VOLTAGE : 0 TO 100V D.C.
OUTPUT CURRENT : 0 TO 2 AMPS D.C.
INPUT VOLTAGE : 4.9V TO 5.1V FULL RANGE CONTROL (R_6=0)
INPUT CURRENT : 0 TO 50µA
POWER GAIN : 20,000,000

Fig 40 High gain proportioning control - D.C output

13 A C. STATIC SWITCHING

It is frequently desirable to use the CS or SCR to provide on-off switching of power to a load In these applications the contact making actuator only has to supply the gate firing current and voltage If the actuating element is a set of mechanical contacts many advantages can be realized compared to the case where the mechanical contacts actually switch the load power Contact voltage and current can be established at any desired level for maximum contact life Also, much more sensitive contacts can be used Some of the applications in which this type of static switching could be useful are counting, sorting, speed governors, temperature control and safety devices

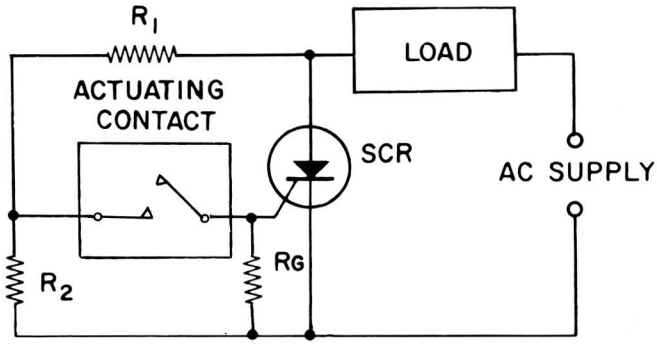


Fig 41

A half wave output static switching circuit is shown in Figure 41 Control voltage is derived from the AC line R_1 and R_2 limit contact voltage and current to any preset level If gate to cathode voltage applied to the SCR, during the reverse half cycle, exceeds the -5 volt rating, a diode should be connected between gate and cathode to limit negative gate voltage A separate gate source voltage could be used if desired rather than obtaining gate voltage from the AC line The circuit as shown turns on power when the contacts are closed Figure 42 shows the reverse case Power is on with the contacts open and off with the contacts closed In both cases the dropping resistor R_1, needs only supply enough current to meet the firing requirements of the SCR.

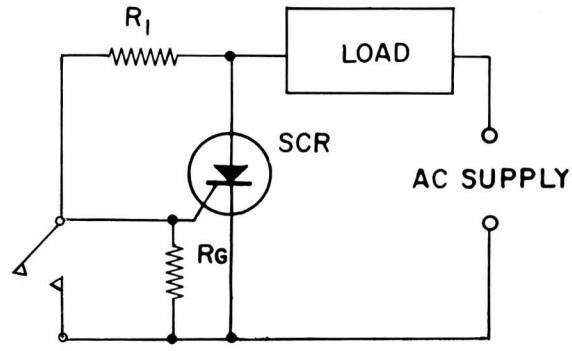


Fig 42

A full wave A C output static switch is shown in Figure 43 A bridge rectifier supplies full wave D C for the control circuit Isolating diodes D_1 and D_2 are necessary in the gate circuit since the gates are tied into opposite sides of the AC line

A circuit supplying full wave D C to the load is easily constructed using the basic circuit shown in Figure 9

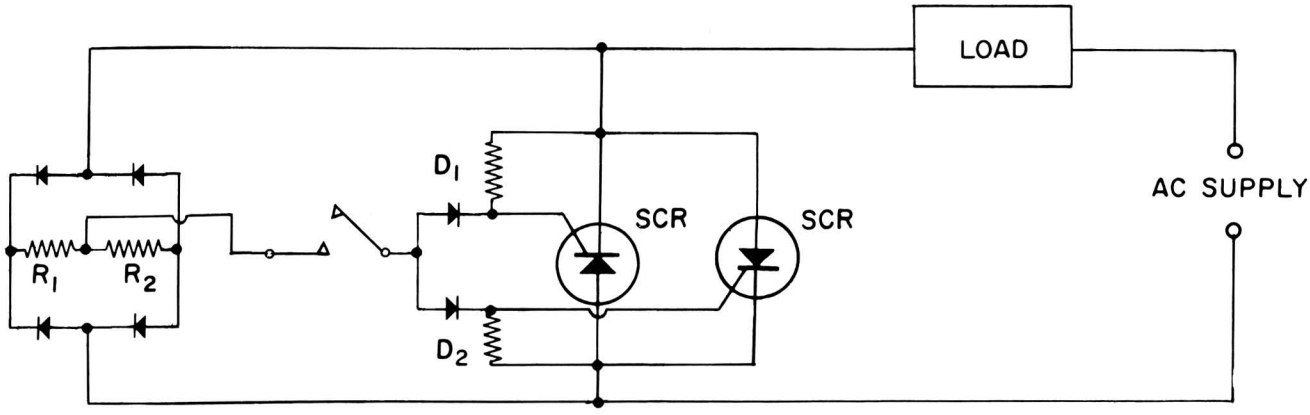


Fig 43

14 D C TO D C. CONVERTERS

The CS or SCR offer several advantages in D C to D C converters or in D C to A. C inverters They have high switching efficiency, high current handling ability, along with miniature size They can also be operated at ultrasonic frequencies and therefore reduce the step-up transformer size

Generally, D C to D C conversion is accomplished by transforming the D C source to AC, stepping up the AC through a transformer, then rectifying the AC output to D C

There are two approaches to achieving D. C to AC inversion. One is the series inverter which is a current generator, and the other is the parallel inverter which is a voltage generator Figures 44 and 45 show a basic approach to each of these methods

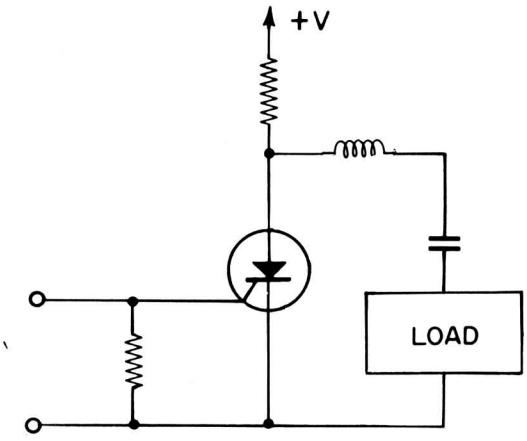


Fig 44 Series inverter

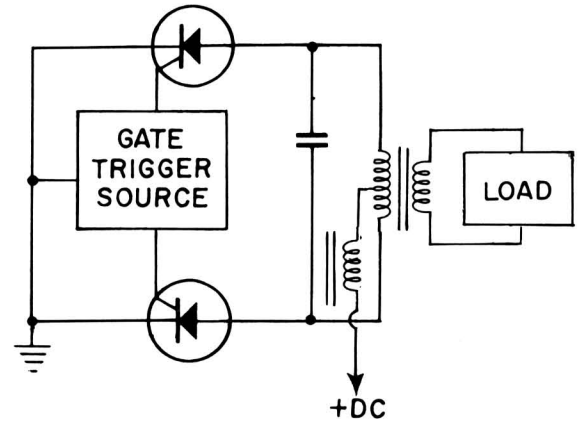


Fig 45 Parallel inverter

15 SERVOMOTOR DRIVING

Servomotor drive circuits can take on many forms depending upon the application requirements The proportioning control circuit in Figure 39 is one approach. This will provide a D C output voltage in proportion to an input error voltage with very high gain Intermediate amplifier stages between the error signal source and the input to this circuit are usually unnecessary This circuit will provide D C output power up to 200 watts and its physical size can be made very small Since it operates off the AC line, a separate D C power supply, as may be required with transistor output stages, is unnecessary

Where a reversing drive is necessary, two of these amplifiers can be used, one for each direction A balanced bridge input between the two amplifiers would provide an input signal to the correct amplifier depending upon the polarity of the error signal

For simple AC systems, the output circuit in Figure 46 could be used This provides a constant amplitude A. C sine wave output with reversible phase It is therefore a reversing drive for AC motors The load voltage will either be in phase or 180° out of phase with the supply voltage depending on whether the control AC input is in phase or 180° out of phase with the supply

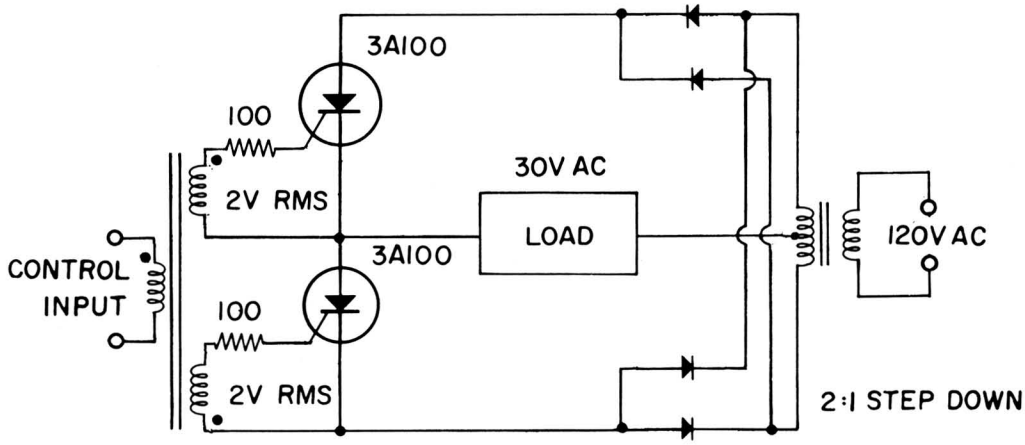


Fig. 46 A C reversing drive

16 CONCLUSION

Many circuit applications for the CS and the SCR have been covered in this Bulletin. These represent the most common uses at the present time, yet are by no means all inclusive for these versatile components It is expected that new applications areas will develop as the "state of the art" of circuit design advances The creative design engineer will find the CS and the SCR practical and useful active elements in the systems design problems he now faces as well as those that will arise in the future

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