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An Introduction to COS/MOS Integrated Circuits and their Applications in Digital-Circuit Systems

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AN INTRODUCTION TO COMPLEMENTARY-SYMMETRY MOS INTEGRATED CIRCUITS AND THEIR APPLICATIONS IN DIGITAL-CIRCUIT SYSTEMS

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Monolithic integrated circuits containing p-channel and n-channel MOS transistors are excellently suited for digital-circuit applications. RCA has been a pioneer in the processing and design technology that has led to the creation of a new family of unique monolithic integrated circuits utilizing complementary-symmetry MOS (COS/MOS) transistors in configurations which encompass both logic and memory. The commercial availability of COS/MOS circuits now makes possible dramatic new innovations in digital-equipment design, performance, and applications.

COS/MOS logic and memory circuits offer micropower quiescent operation, moderately fast propagation delay, excellent noise immunity, large fan-out capability, and operation from a single power supply over a wide voltage range. The characteristics of COS/MOS logic and memory circuits are comparatively immune to variations in temperature and are rated for operation over the full military temperature range of -55°C to +125°C. COS/MOS circuits of Medium-Scale Integration (MSI) complexity operate with simple single-phase clocking. Engineering research indicates that COS/MOS circuits also show great promise for future use in Large-Scale Integration (LSI).

This paper describes a total of nine different COS/MOS circuit configurations, ranging from compatible gates to flip-flops and simple arrays that interface directly with MSI logic and memory circuits. COS/MOS circuits are ideal for a broad spectrum of applications in digital-circuit systems.

THE BASIC COS/MOS INVERTER CIRCUIT

The basic COS/MOS inverter circuit is shown in Fig.1(a). This monolithic circuit consists of one p-channel enhancement-type MOS transistor and one n-channel enhancement-type MOS transistor, with their drains tied in common and effectively operating in a "series" connection from a single power supply. The logic-swing gate voltage ranges from zero to the supply voltage V. When the voltage of + V (e.g., logical "1") is applied at the input, the n-channel unit is turned ON and the p-channel unit is turned OFF; the output is then in the low state (logical "0"), and logic-voltage inversion has been accomplished, as illustrated by the curve in Fig.1(b). When zero voltage (e.g., logical "0") is applied at the input, the p-channel unit is turned ON and the n-channel unit is turned OFF. This inverter action results in an output of +V volts (logical "1"), as shown in the curve of Fig.1(c).

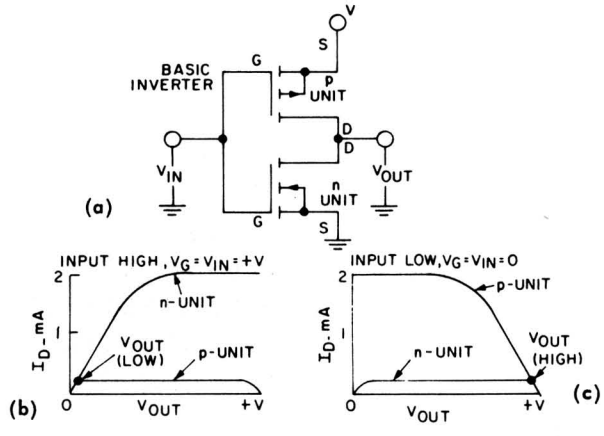

Fig.1 - Basic COS/MOS inverter.

It should be understood that in either logic state one unit is OFF while the other is ON. Consequently the quiescent power dissipation is simply the product of the OFF-unit leakage current and the supply voltage.

Because the OFF-unit leakage current is typically about 10 nanoamperes at a drain-to-source voltage of 10 volts, the quiescent power dissipation for the simple inverter is typically about 10 nanowatts in either logic state.

The input impedance of the typical COS/MOS transistor pair is extremely high, typically 10^{12} ohms. This high-input-impedance characteristic permits fan-out of COS/MOS pairs without significant increase of the low quiescent power consumption. Furthermore, there are essentially no dc restrictions on fan-out capability (i.e., the circuits have infinite fan-out capability). Although fan-out does increase the capacitance loading and thus reduces speed, the practical fan-out capability can be greater than 50.

During switching, when the capacitance in the output circuit (including the load) must be charged up to the "high" level through the ON p-channel transistor, additional power is dissipated in the p-channel unit. Furthermore, the charge stored in the output and load capacitance is dissipated in the n-channel transistor when the input goes "high". The dynamic power P required for switching is given by

$$P = C_o V_{DD}^2 f \qquad (1)$$

where C_o is the capacitance at the output node, V_{DD} is the supply voltage, and f is the frequency in hertz. Fig.2 shows the power dissipation as a function of frequency for the inverter circuit of Fig.1(a). It is apparent that COS/MOS circuits can be operated very efficiently because their quiescent power consumption is low and their dynamic power consumption is directly related to the switching rate required. In this respect, COS/MOS circuits have a kinship with a magnetic core operating in a memory system because the core dissipates power only during each switching transient, but not in the quiescent "1" or "0" states.

COS/MOS circuits have inherently sharp transfer characteristics, as shown in Fig.3 for the simple inverter of Fig.1. As a consequence, the noise immunity of the logic circuits is typically about 40 per cent of the power-supply voltage (e.g., 4 volts for a V_{DD} of 10 volts). Fig.3 also shows the comparatively minor variations in transfer characteristics at the extremes of the operating-temperature range. The COS/MOS circuits make excellent switches because their extremely low saturation voltage (typically less than one millivolt) results in very large ratios of "off" to "on" output voltages. In addition they exhibit a low "1"- and "0"-level output impedance, typically 1000 ohms with a 10-volt supply.

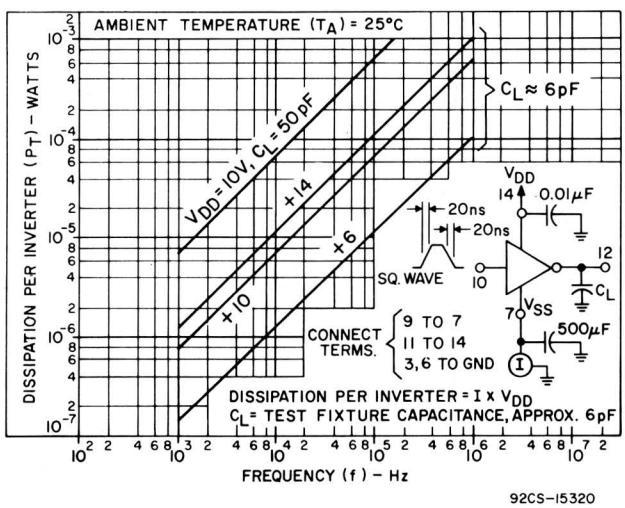

Fig.2 - Typical dissipation characteristics of basic COS/MOS inverter circuit.

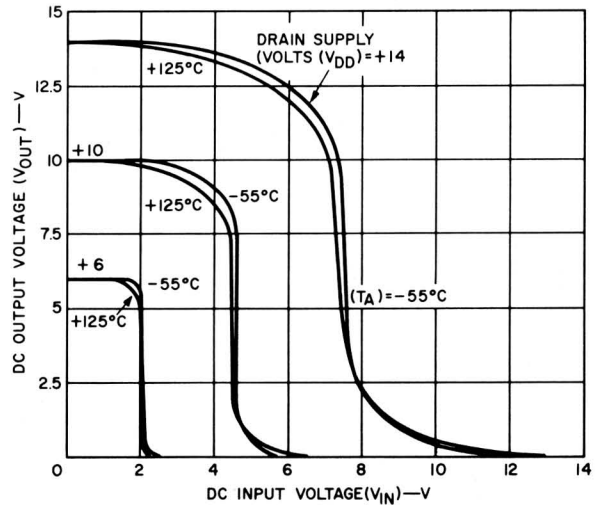

Fig.3 - Typical transfer characteristics for COS/MOS circuits (inverter, NOR, NAND) with variations over temperature range.

A SIMPLE ARRAY OF COS/MOS TRANSISTORS

The simple array of COS/MOS transistors shown in Fig.4 is composed of three n-channel and three p-channel enhancement-type MOS transistors on a single monolithic silicon chip. The COS/MOS pair of transistors at the right side of Fig.4 is connected as an inverter in a configuration identical to that shown in

Fig.1. A second inverter can be made available by interconnection of terminals 8 and 13, and a third inverter configuration can be provided by interconnection of terminals 1 and 5. This trio of inverters is one of numerous COS/MOS logic-circuit arrangements which can be designed with the basic CD4007 circuit.

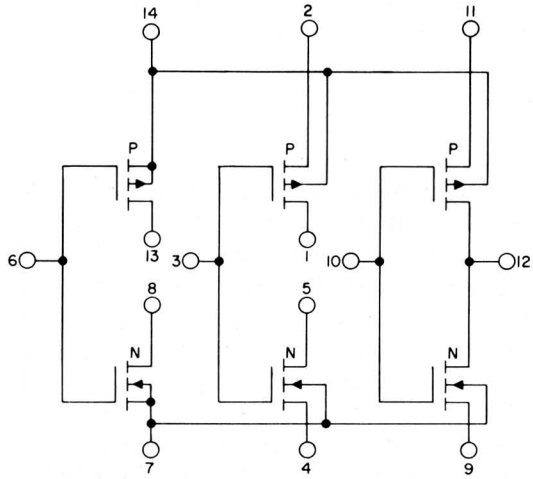

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Fig.4 - Schematic diagram of COS/MOS array consisting of dual transistor pairs plus inverter (CD4007 14-lead ceramic flat package; CD4007D 14-lead dual-in-line ceramic package).

Typical and "minimum" drain characteristics for the COS/MOS transistors in the CD4007 array of Fig.4 are shown in Fig.5. At first glance, it might appear that such a spread of characteristics would be intolerable in a practical device. However, these data serve to underscore another attribute of COS/MOS circuits,

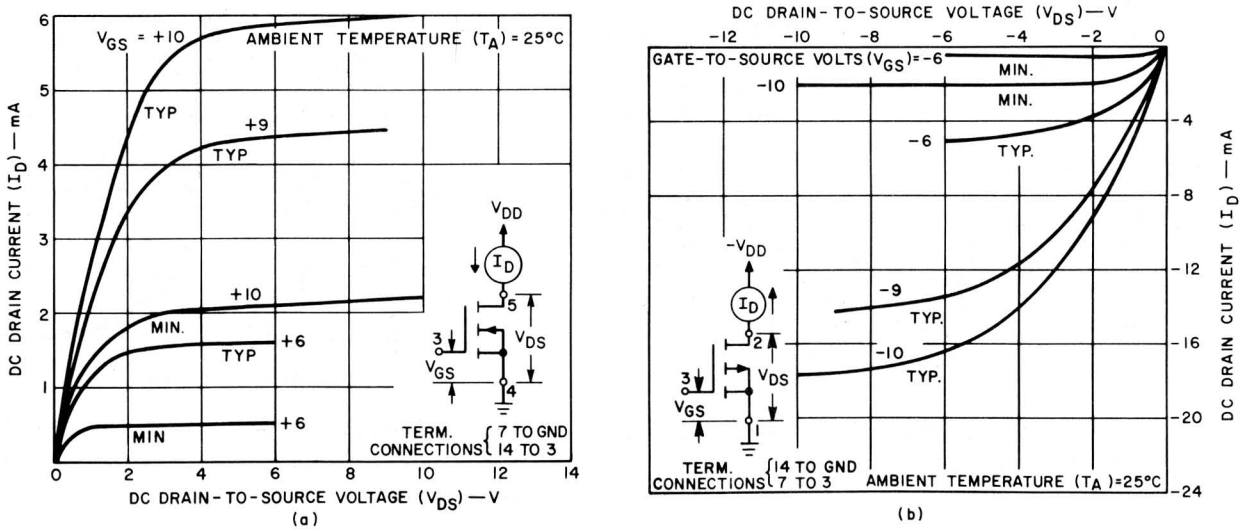


Fig.5 - Typical and minimum drain characteristics for (a) n-channel and (b) p-channel transistors in array of Fig.4.

i.e., they offer enhanced reliability over long periods of time because the output logic levels of the circuits are essentially equal to the power-supply voltages and are relatively independent of device threshold-voltage or transconductance variations. In addition, the circuits are operationally tolerant of wide variations in supply voltage (e.g., 6 to 15 volts in the case of the CD4007). Typical "turn-on" characteristics for COS/MOS transistors as a function of supply voltage are shown in Fig.6.

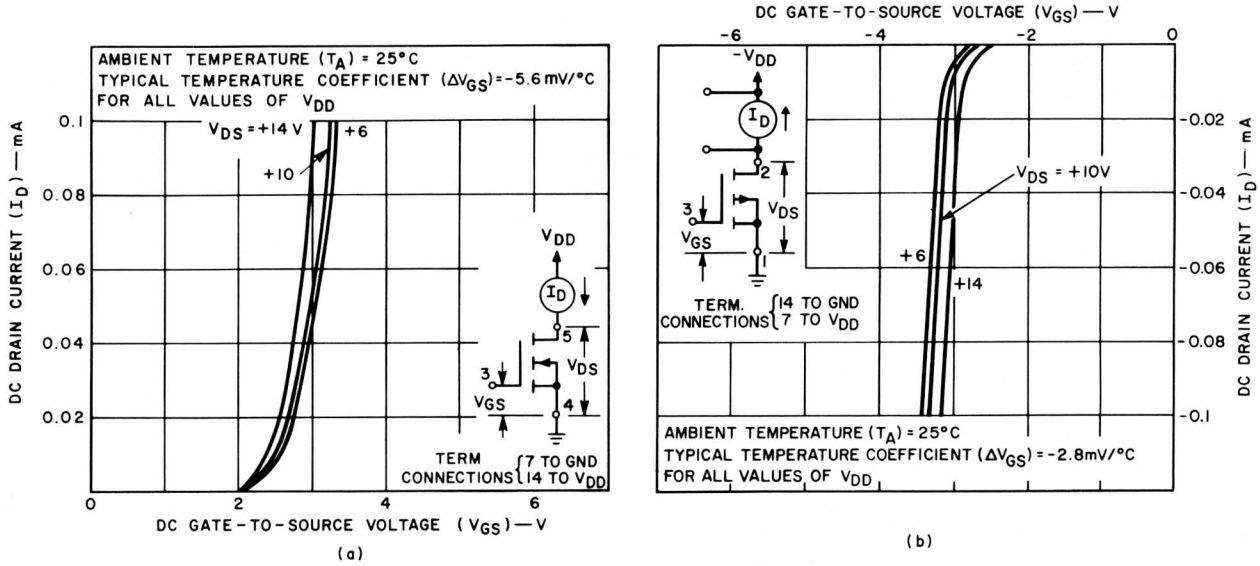


Fig.6 - Typical turn-on characteristics for (a) n-channel and (b) p-channel transistors in array of Fig.4.

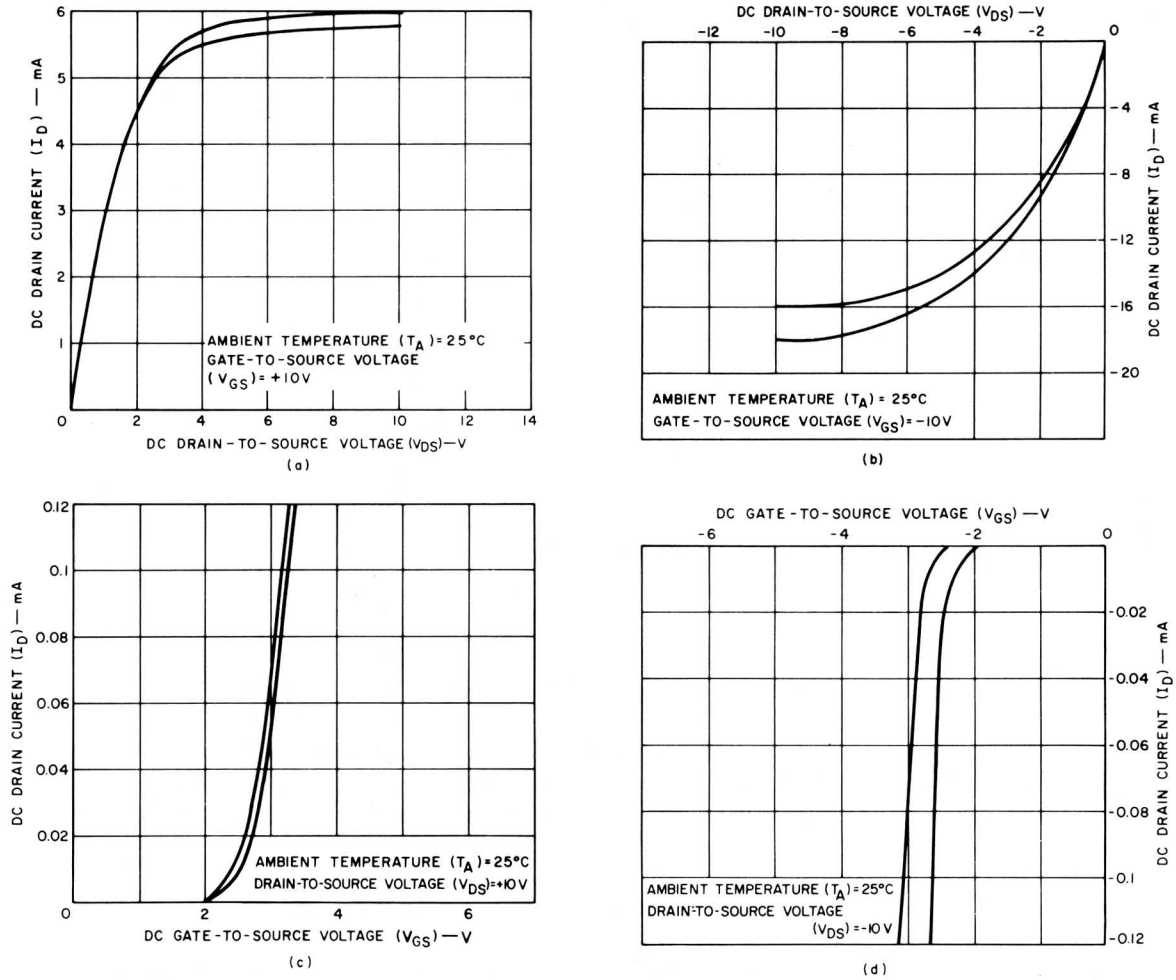


Fig.7 - Typical matching of characteristics for any two units in the array of Fig.4: (a) n-channel drain characteristics; (b) p-channel drain characteristics; (c) n-channel turn-on characteristics; (d) p-channel turn-on characteristics.

Because the CD4007 COS/MOS array transistors are of monolithic construction and are fabricated on the same chip at the same time, their characteristics are closely matched. Typical characteristics matching for any two similar-channel-type units on the same chip is illustrated in Fig.7. Fig.8(b) shows the propagation-delay waveforms for the CD4007 as measured in the test setup of Fig.8(a). Fig.9 shows propagation-delay and transition-time characteristics as a function of load-capacitance (C_L) values up to 100 picofarads. The input capacitance of each COS/MOS pair in the CD4007 is typically 5 picofarads.

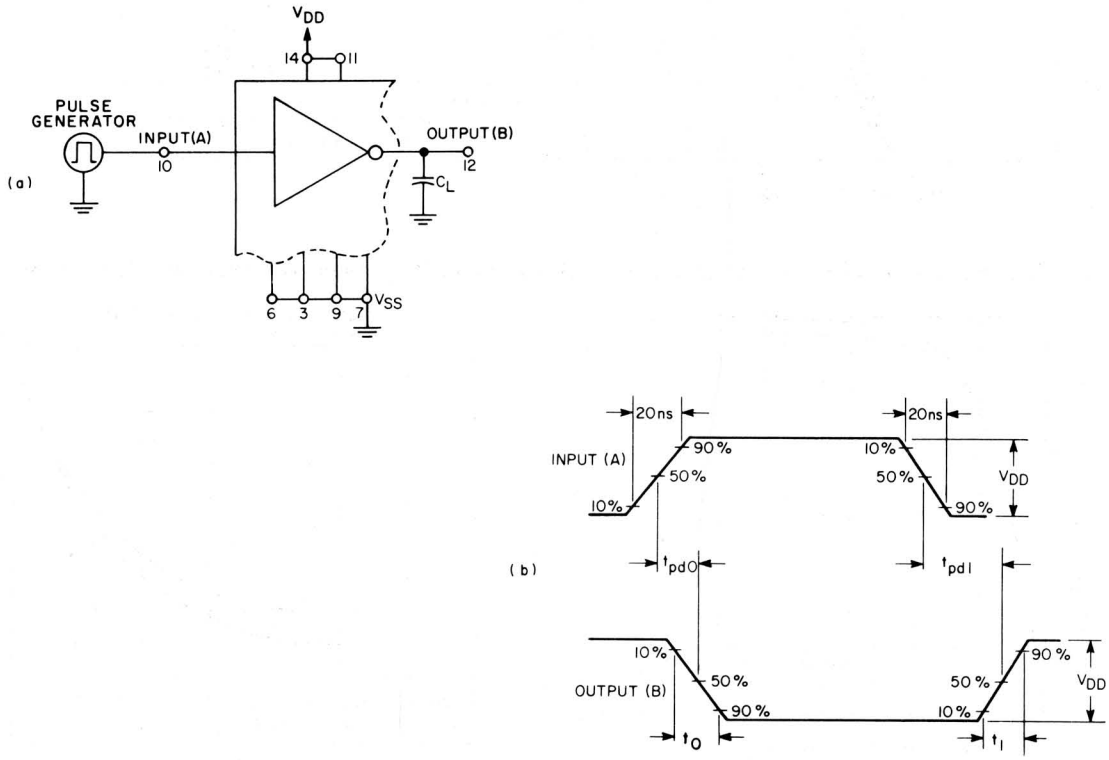


Fig.8 - Propagation delay test setup and waveforms for the array of Fig.4.

Typical Logic Circuit Arrangements for the Simple COS/MOS Array

Fig.10 shows eight typical circuit arrangements for the simple CD4007 COS/MOS array shown in Fig.4. More complex functions are possible by the use of multiple packages. The versatility of this simple array makes it possible to customize a variety of COS/MOS circuits, including inverters, NOR gates, RS flip-flops, transmission gates, NAND gates, as others.

NOR POSITIVE LOGIC WITH LOW-POWER COS/MOS GATES

Fig.11 shows the schematic diagrams, logic diagrams, and logic equations for three low-power COS/MOS gate circuits for NOR positive-logic applications. These circuits have characteristics essentially similar to those of the CD4007. They are capable of medium-speed operation, e.g., a typical propagation delay time of 50 nanoseconds with a load capacitance of 15 picofarads. Their design flexibility, high noise immunity, and ability to operate with a fairly unregulated power supply make these circuits ideal for use as "building blocks" in a wide variety of computer peripheral equipments.

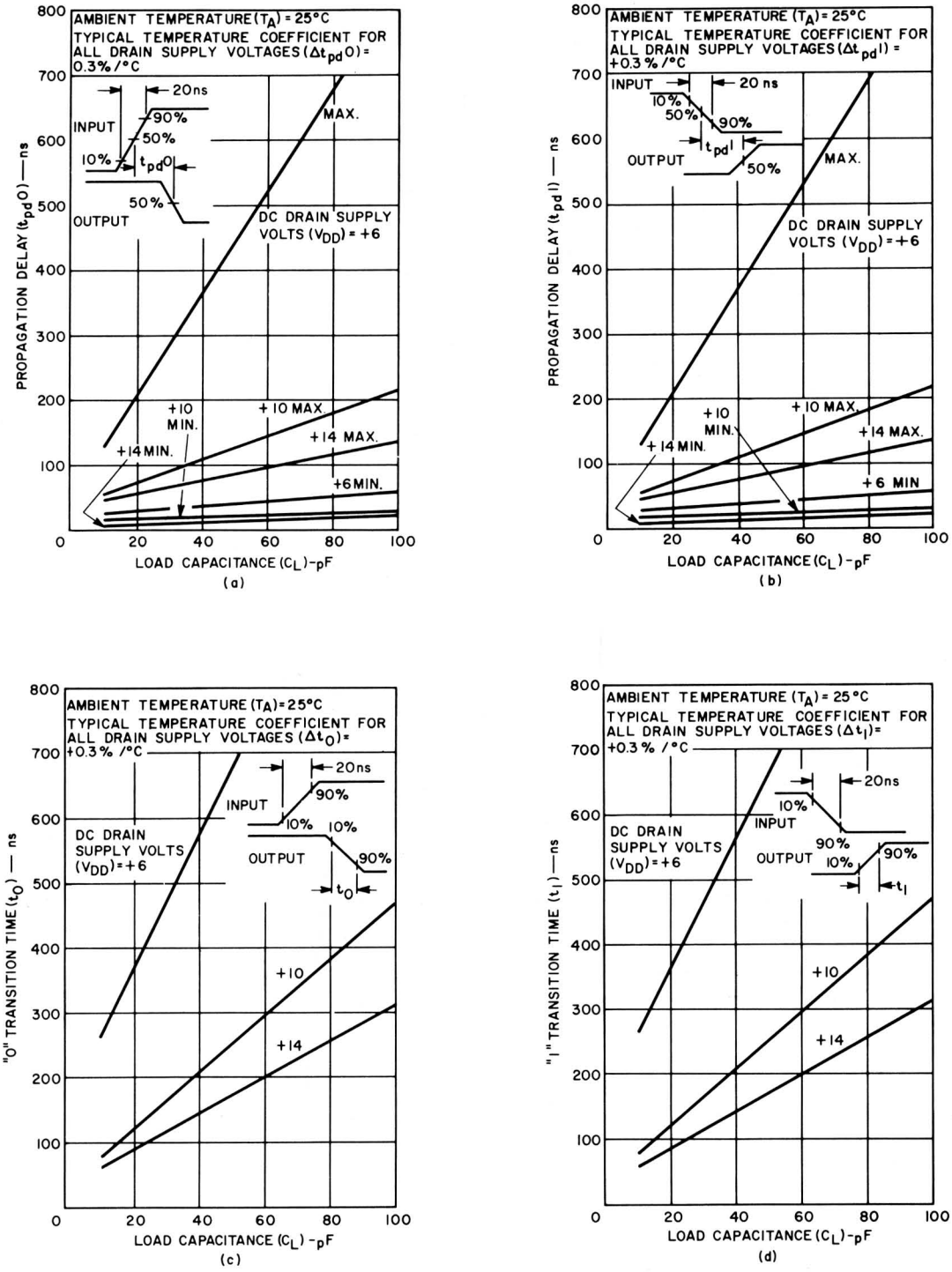
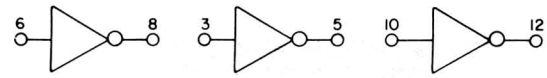
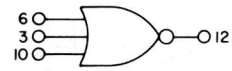


Fig.9 - Propagation-delay and transition-time characteristics for COS/MOS transistors used in the array of Fig.4; (a) "zero" propagation delay; (b) "one" propagation delay; (c) "zero" transition time; (d) "one" transition time.

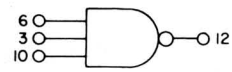
a) Triple Inverters



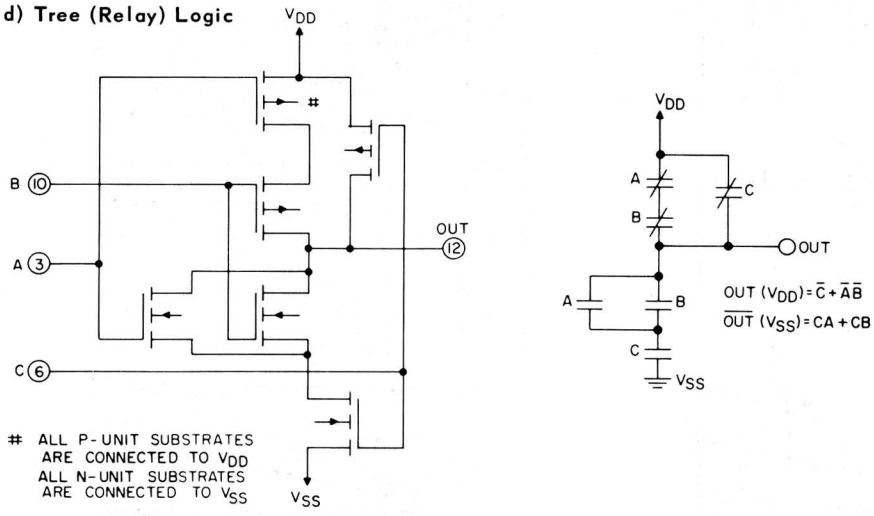
b) 3-Input NOR Gate



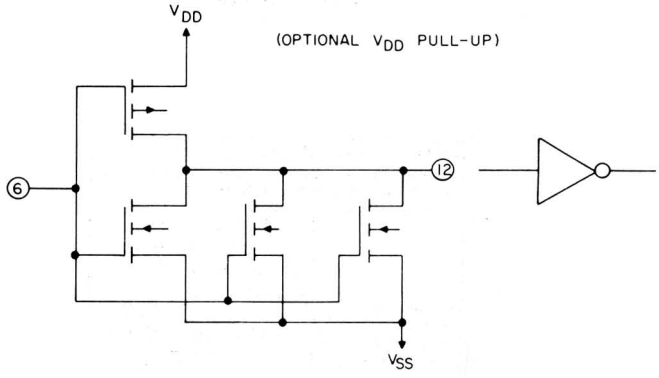
c) 3-Input NAND Gate



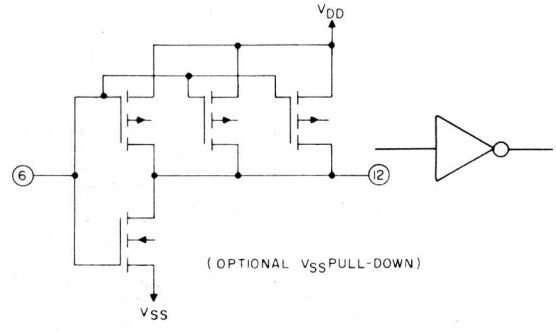
d) Tree (Relay) Logic



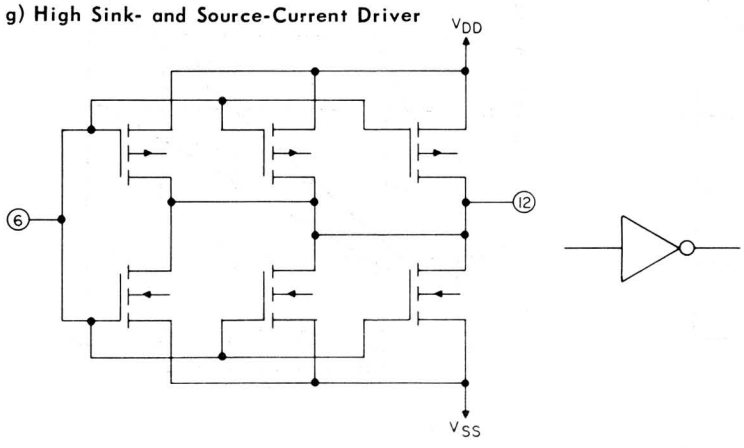
e) High Sink-Current Driver



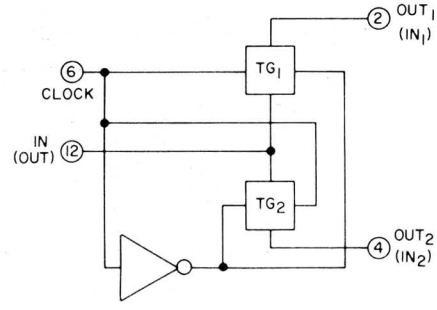
f) High Source-Current Driver



g) High Sink- and Source-Current Driver

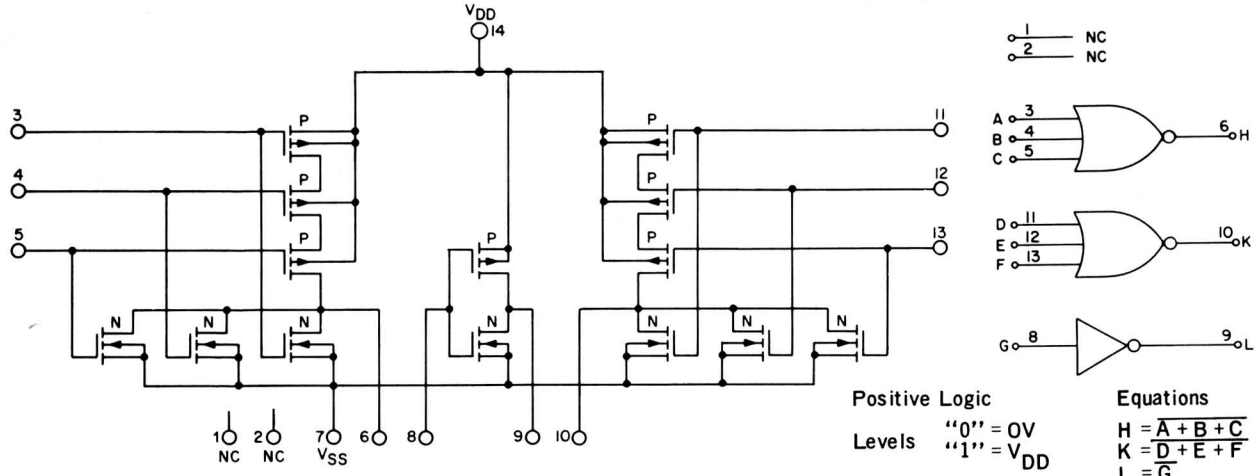


h) Dual Bi-Directional Transmission Gating

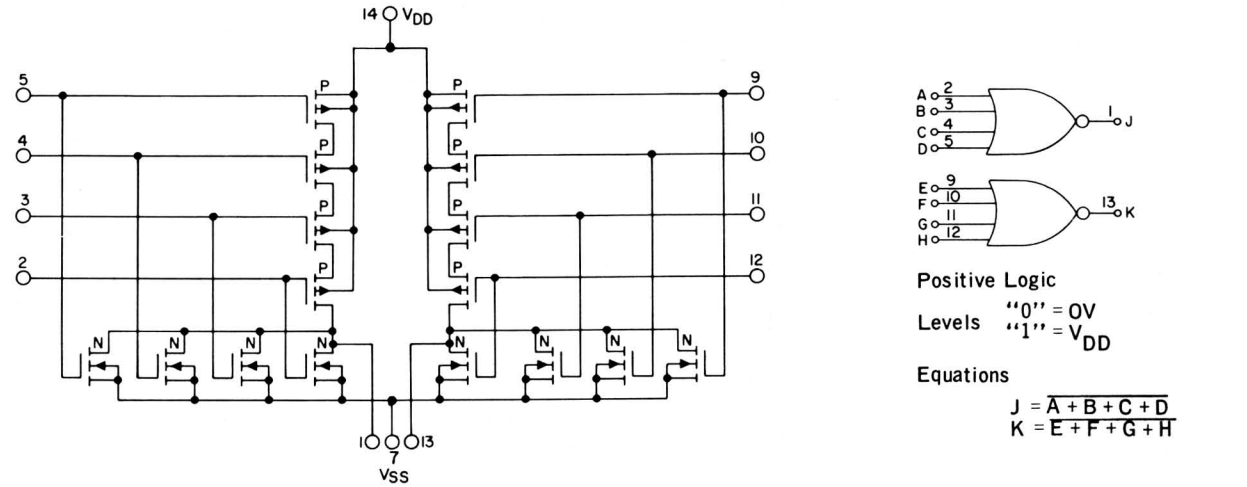


Notes: $V_{SS} \leq V_{IN} \leq V_{DD}$; V_{IN} = Terminals 3, 6, 10.
Minimum Recommended Power-Supply Voltage ($V_{DD} - V_{SS}$)..... 6 V

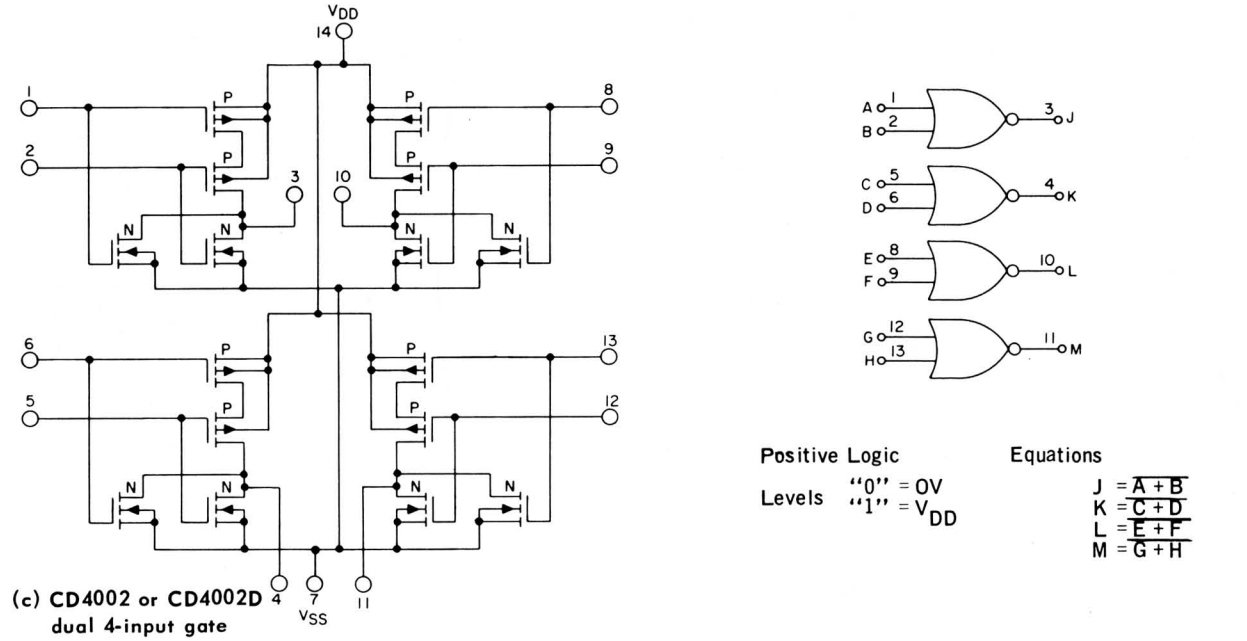
Fig.10 - Typical COS/MOS logic-circuit arrangements using the array of Fig.4.



(a) CD4000 or CD4000D dual 3-input gate plus inverter



(b) CD4001 or CD4001D quad 2-input gate

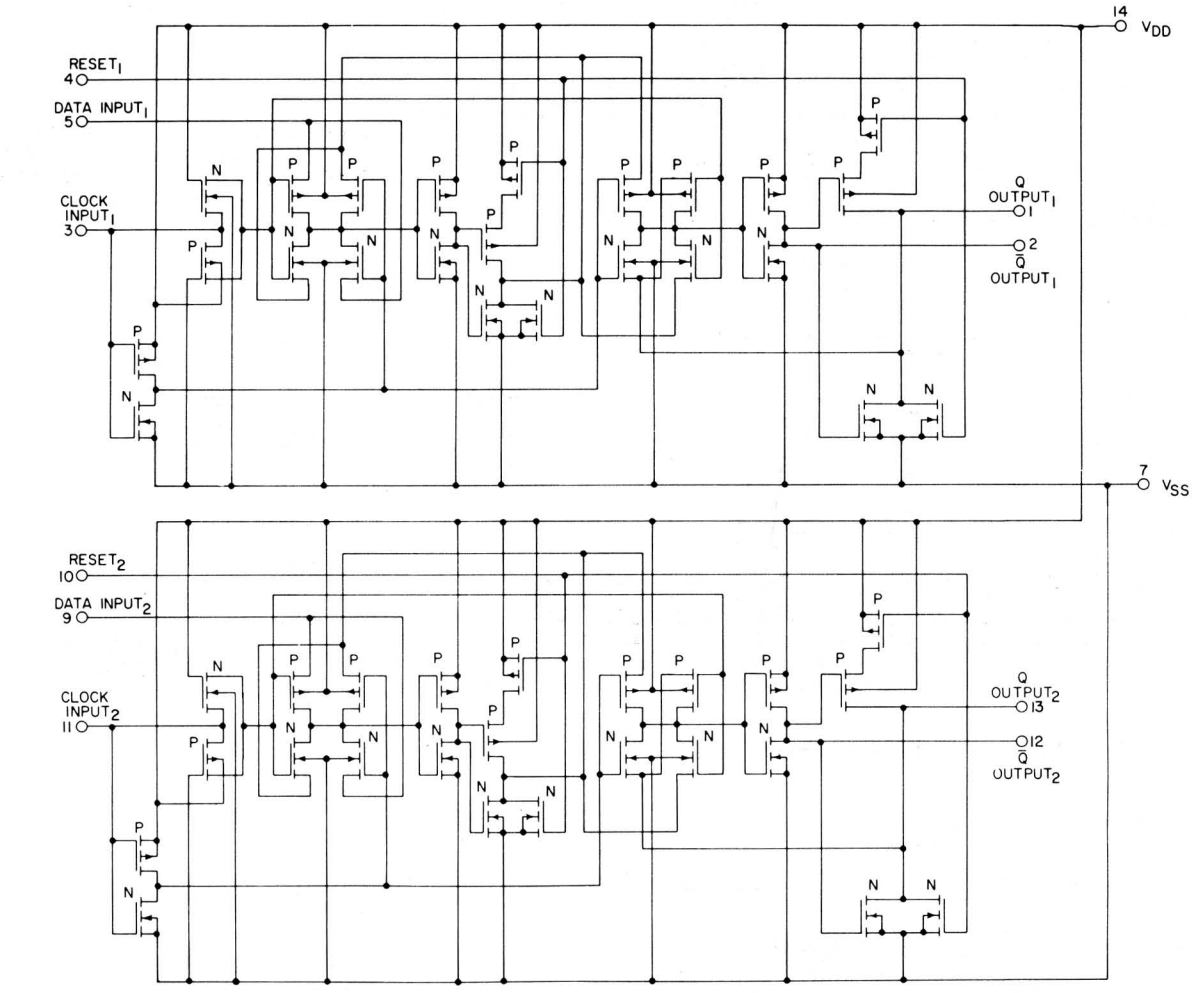


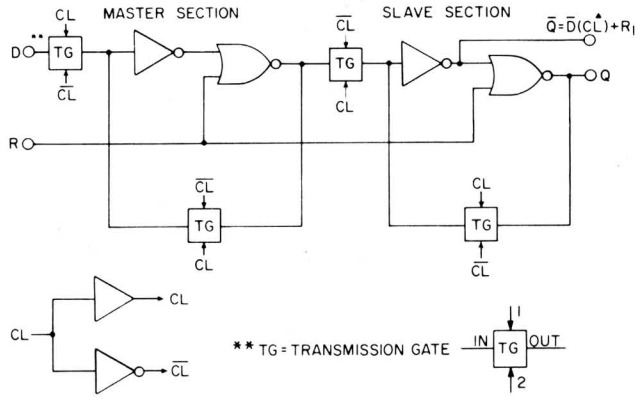
(c) CD4002 or CD4002D dual 4-input gate

Fig.11 - Three low-power COS/MOS gate circuits for NOR positive-logic applications.

A DUAL D-TYPE FLIP-FLOP COS/MOS CIRCUIT

Figure 12 shows the schematic diagram, logic block diagram, and truth tables for the RCA CD4003 or CD4003D Dual D-Type Flip-Flop COS/MOS circuit. The circuit consists of two identical, independent, data-type flip-flops on a single monolithic chip. Each flip-flop has independent data, reset, and clock inputs and





INPUT TO OUTPUT IS:

a) A bidirectional short circuit when control input 1 is "Low" and control input 2 is "High"

b) An open circuit when control input 1 is "High" and control input 2 is "Low"

RESET FUNCTION (DOMINATING)

R	Q	Q̄
0	Q	Q̄ (NO CHANGE)
1	0	1

D, CL OPERATION (WITH R=0 V)

D	CL▲	Q	Q̄
0	⌐	0	1
1	⌐	1	0
X	⌙	Q	Q̄ (NO CHANGE)

▲-LEVEL CHANGE
X-DON'T CARE CASE

Fig.12 - Schematic diagram, logic block diagram, and truth tables for a dual D-type flip-flop COS/MOS circuit (CD4003 14-lead ceramic flat package; CD4003D 14-lead dual-in-line ceramic package).

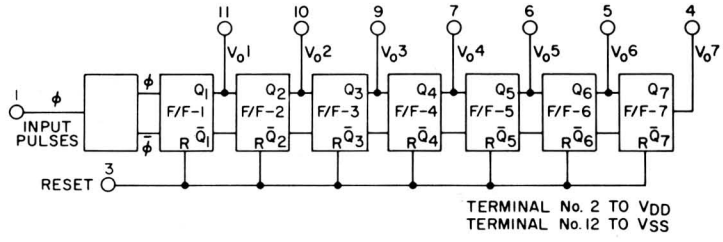
complementary outputs. These devices can be used for shift-register applications and, by connection of the "Q" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the "Q" output during the positive-going transition of the clock pulse. In static flip-flop operation, the circuit retains its state indefinitely with the clock level either high or low.

The characteristics of the CD4003 or CD4003D flip-flops can be summarized as follows:

- Quiescent power dissipation per package (V_{DD}=10 V) ..... 50 (typ) nW
- "0" Propagation Delay (V_{DD} = 10V) (C_Q=$C_{\overline{Q}}$=30pF) ..... 190 (typ) ns
- "1" Propagation Delay (") (") ..... 190 (typ) ns
- "0" Transition Time (") (") ..... 130 (typ) ns
- "1" Transition Time (") (") ..... 130 (typ) ns
- Clock-Pulse Frequency (V_{DD} = 10V) (") ..... 2.5 (max) MHz
  (V_{DD} = 14V) (") ..... 3.6 (max) MHz
- Clock-Pulse Rise and Fall Times (V_{DD} = 10V) (") ..... 5 (max) μs
- Reset Propagation Delay Time
  Reset Q (V_{DD} = 10V) (") ..... 190 (max) ns
  Reset $\overline{Q}$ (") (") ..... 385 (max) ns
- Reset Pulse Duration (") (") ..... 385 (min) ns
- DC Reset Capability
- Input Capacitance (Clock, Data Input, and Reset Lines) ..... 4 to 6 (typ) pF

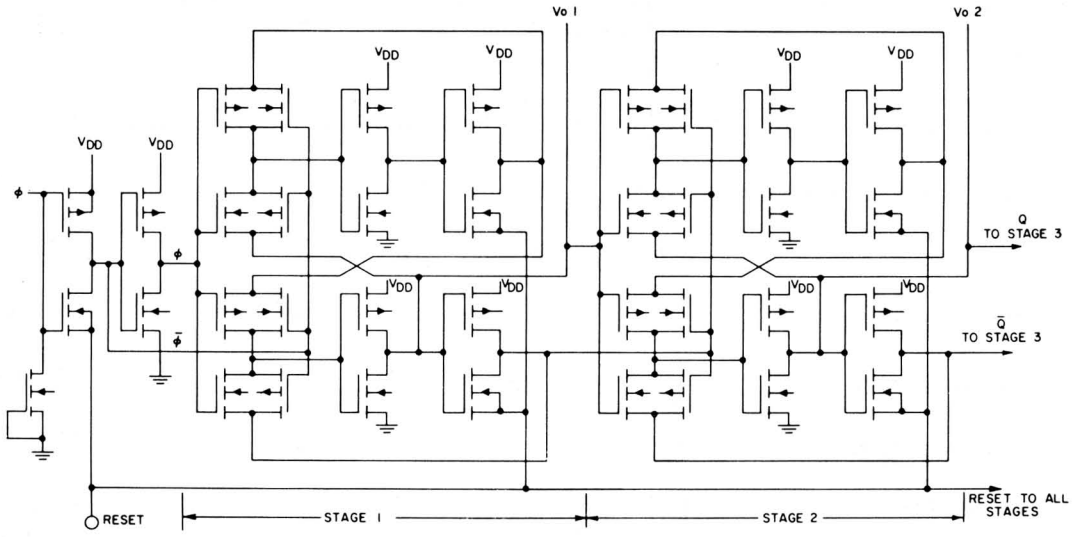
A 7-STAGE LOW-POWER COS/MOS BINARY COUNTER OF THE RIPPLE-CARRY TYPE
MSI (Medium-Scale Integration)

The 7-stage binary-counter frequency-divider configuration shown in Fig.13 is an example of medium-scale integration (MSI) with COS/MOS circuitry. This circuit (RCA CD4004 or CD4404T) is composed of 58 n-channel and 58 p-channel enhancement-type MOS transistors connected to form a pulse-input-shaping circuit and seven ripple-carry binary-counter stages. Resetting of the counter to the all-zero state is accomplished by a high level on the reset line. A master-slave flip-flop configuration is utilized for each counter stage. The state of the counter is advanced one step in binary order on the negative-going transition of the input pulse. In static counter operation, the counter retains state indefinitely with the input-pulse level low or high. This circuit arrangement is particularly suited to frequency-divider, time-delay, and counter control applications.



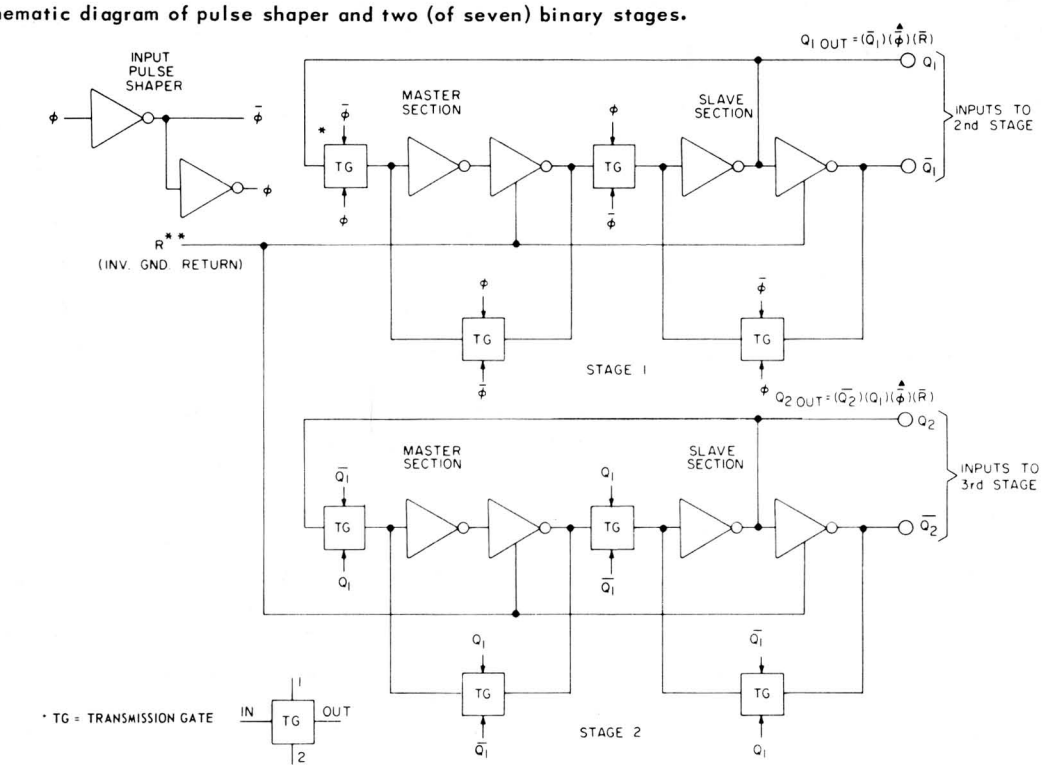
(a) Functional Diagram

Fig.13 (Cont'd)



NOTE: SUBSTRATES FOR ALL "P" UNITS ARE CONNECTED TO V_{DD}
SUBSTRATES FOR ALL "N" UNITS, UNLESS OTHERWISE SHOWN, ARE CONNECTED TO GROUND.

(b) Schematic diagram of pulse shaper and two (of seven) binary stages.



$Q_{1\,OUT} = (\bar{Q}_1)(\overset{\blacktriangle}{\Phi})(\bar{R})$

$Q_{2\,OUT} = (\bar{Q}_2)(Q_1)(\overset{\blacktriangle}{\Phi})(\bar{R})$

EQUATIONS FOR STAGES 3 TO 7

$Q_{3OUT} = (\bar{Q}_3)(Q_1)(Q_2)(\overset{\blacktriangle}{\Phi})(\bar{R})$

$Q_{4OUT} = (\bar{Q}_4)(Q_1)(Q_2)(Q_3)(\overset{\blacktriangle}{\Phi})(\bar{R})$

$Q_{5OUT} = (\bar{Q}_5)(Q_1)(Q_2)(Q_3)(Q_4)(\overset{\blacktriangle}{\Phi})(\bar{R})$

$Q_{6OUT} = (\bar{Q}_6)(Q_1)(Q_2)(Q_3)(Q_4)(Q_5)(\overset{\blacktriangle}{\Phi})(\bar{R})$

$Q_{7OUT} = (\bar{Q}_7)(Q_1)(Q_2)(Q_3)(Q_4)(Q_5)(Q_6)(\overset{\blacktriangle}{\Phi})(\bar{R})$

INPUT TO OUTPUT IS

a) A BIDIRECTIONAL SHORT CIRCUIT WHEN CONTROL INPUT 1 IS "LOW" AND CONTROL INPUT 2 IS "HIGH"

b) AN OPEN CIRCUIT WHEN CONTROL INPUT 1 IS "HIGH" AND CONTROL INPUT 2 IS "LOW"

** R = HIGH DOMINATES (RESETS ALL STAGES)

▲ACTION OCCURS ON NEGATIVE GOING TRANSITION OF INPUT PULSE. COUNTER ADVANCES ONE BINARY COUNT ON EACH NEGATIVE Φ TRANSITION (128 TOTAL BINARY COUNTS)

(c) Logic block diagram for input pulse shaper and two (of seven) binary stages, together with logic equations for the seven stages.

Fig.13 - Functional diagram, partial schematic diagram, partial logic block diagram, and logic equations for a 7-stage low-power COS/MOS binary counter of the ripple-carry type (CD4004 14-lead ceramic flat package; CD4004T 12-lead TO-5-style package).

The characteristics of the CD4004 or CD4004T binary counter/frequency divider array can be summarized as follows:

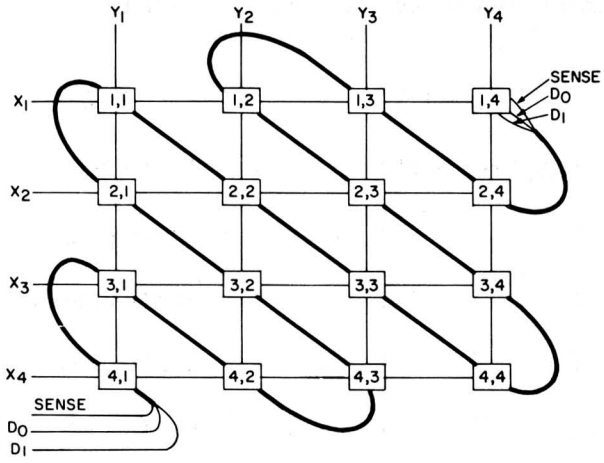
- Quiescent power dissipation (V_{DD} = 14V) ..... 5 (typ) μW
- "0" Propagation Delay (V_{DD} = 10V) (C_{Q1}-C_{Q7}=30 pF) ..... 175 (typ) ns
- "1" Propagation Delay (") (") ..... 190 (typ) ns
- "0" Transition Time (") (") ..... 150 (typ) ns
- "1" Transition Time (") (") ..... 225 (typ) ns
- "0" Input-Pulse Duration (") (") ..... 600 (min) ns
- "1" Input-Pulse Duration (") (") ..... 200 (min) ns
- Input-Pulse Frequency (V_{DD} = 10V) (") ..... 1.25 (max) MHz
  (V_{DD} = 14V) (") ..... 2.0 (max) MHz
- Input-Pulse Rise and Fall Times (V_{DD} = 10V) (") ..... 15 (max) μs
- Reset Propagation Delay Time (V_{DD} = 10V) (") ..... 80 (typ) ns
- Reset-Pulse Duration (") (") ..... 400 (min) ns
- Reset Conditions ..... For example, with V_{DD} = 10V the reset line voltage must not exceed 1 volt; for a typical peak current of 2mA, the drive impedance must be $\lesssim$500 ohms.
- Input Capacitance

  ø ..... 3.5 (typ) pF
  Reset ..... 40 (typ) pF

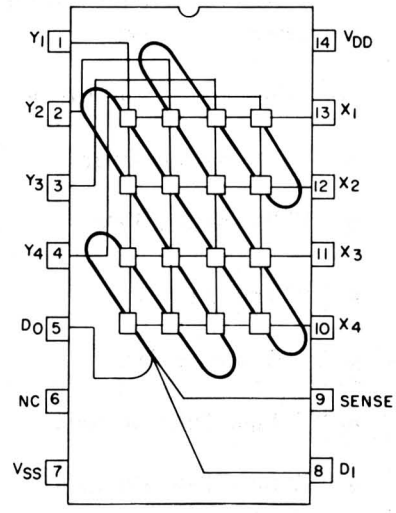
The characteristics of propagation delay, transition time, and input-pulse frequency can be improved markedly if the loading capacitances C_{Q1} to C_{Q7} are reduced. For example, the circuit can operate at an input pulse rate in excess of 2.5 MHz (V_{DD} = 10V) if there is no external capacitive loading on C_{Q1} to C_{Q6}.

A LOW-POWER COS/MOS 16-BIT NDRO-TYPE MEMORY CIRCUIT
MSI (Medium-Scale Integration)

Fig.14 shows diagrams for the RCA CD4005 or CD4005D 16-word, 1-bit-deep, non-destructive-readout (NDRO) memory implemented with COS/MOS transistors. This circuit consists of 16 flip-flop storage cells arranged in an X-Y matrix for easy access, as shown in Fig.14(a) and (b). Each storage cell contains a flip-flop, which consists of two cross-coupled COS/MOS inverter stages, and two transmission gates (also known as bi-directional gates). The schematic diagram of one COS/MOS memory cell in Fig.14(c) shows the connection of two n-channel MOS transistors to perform the transmission gating to and from each cell. Fig.14(d) shows a truth table applicable to each cell.

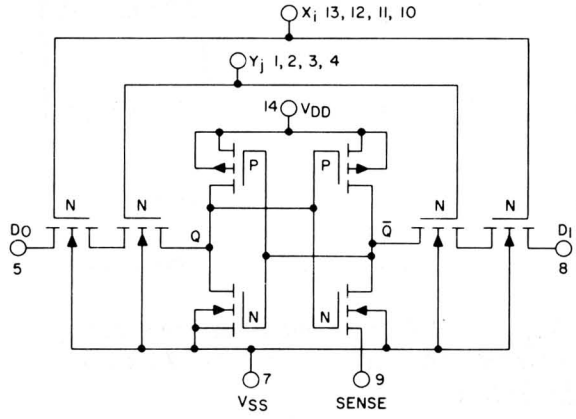


(a) Memory-Cell Arrangement Diagram



NOTE: ALL UNUSED INPUTS MUST BE CONNECTED TO THE MOST NEGATIVE CIRCUIT VOLTAGE (V_{SS}).

(b) Functional Diagram



NOTE: V_{DD}, V_{SS}, D_0, D_1 AND SENSE LINES ARE COMMON TO ALL 16 CELLS.

X_i = X_1 OR X_2 OR X_3 OR X_4

Y_i = Y_1 OR Y_2 OR Y_3 OR Y_4

X AND Y LINES ARE COMMON TO FOUR CELLS EACH AND ARE CONNECTED IN MATRIX FORMAT.

(c) Schematic Diagram – One of 16 Memory Cells

WRITING VIA D_0 and D_1 LINES					
X	Y	D_0	D_1	CELL STATUS	SENSE CURRENT (mA)
0	0	X	X	NC	0
1	0	X	X	NC	0
0	1	X	X	NC	0
1	1	0	0	U	0
1	1	1	0	1	0
1	1	0	1	0	0
CURRENT SENSING AT "SENSE" LEAD					
1	1	1	1	1	0.5
1	1	1	1	0	0
LOGIC-LEVEL SENSING ON D_0 & D_1 LEADS					
1	1	Q	$\bar{Q}$	NC	"sense" line shorted to V_{SS}

(d) Truth Table (Each Cell)

POSITIVE LOGIC

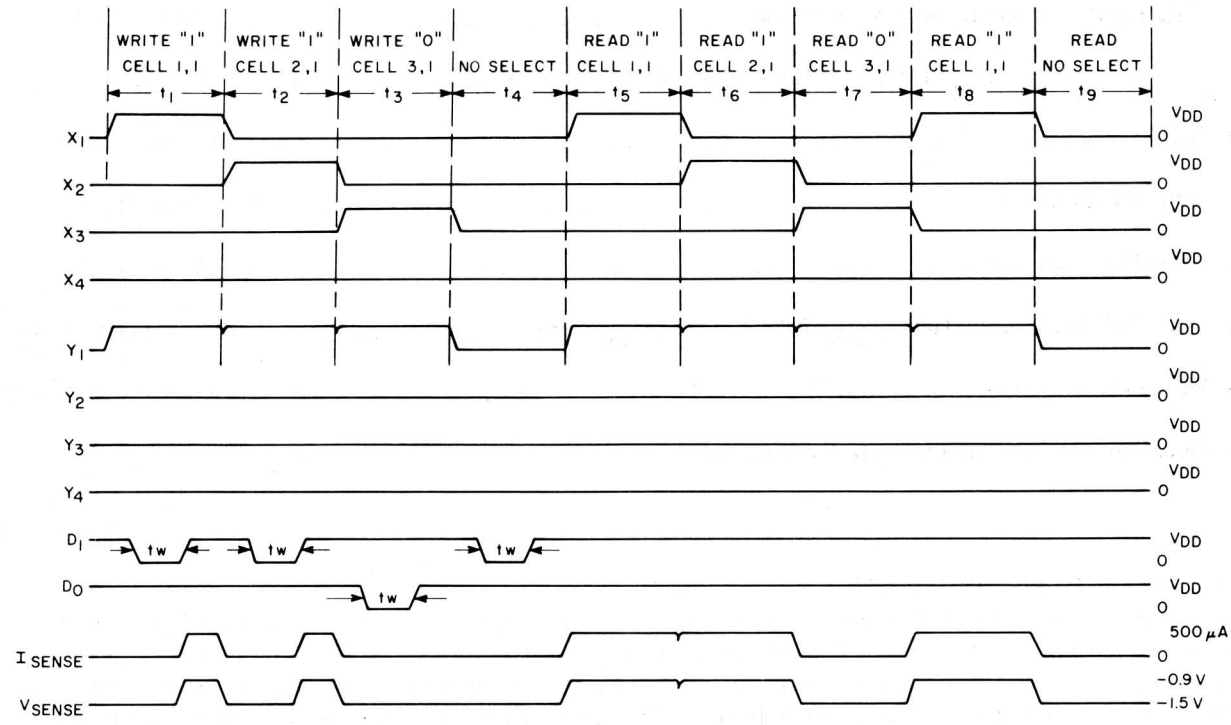
Levels | "0" V_{SS} | "1" V_{DD}

X = DON'T CARE

NC = NO CHANGE

U = UNDETERMINABLE

Fig. 14 (Cont'd)



(e) Typical Timing Diagram

Fig.14 - Memory-cell arrangement diagram, functional diagram, partial schematic diagram, truth tables, and timing diagram for a low-power COS/MOS 16-bit NDRO-type memory circuit (CD4005 14-lead ceramic flat package; CD4005D 14-lead dual-in-line ceramic package).

Mode of Operation

Addressing of a particular cell is accomplished by the simultaneous application of high voltage levels on the X-Y coordinates of that cell. A "1" is written into an addressed cell by the application of a low voltage level on the D_1 line and a high voltage level on the D_0 line; conversely, a "0" is written into the addressed cell by forcing the D_0 line "low" and the D_1 line "high". Nondestructive readout (NDRO), or sensing, at the $\overline{Q}$-sense return line of an addressed cell is accomplished by providing sense current by means of an externally forced high-level voltage on the D_1 line. The D_0 line is also maintained at a high voltage level during readout. Sensing can also be accomplished by external logic-level monitoring of the D_0 and D_1 lines. In this mode of sensing, logic circuitry must be provided that will inhibit the writing operation during readout, and the sense line must be connected to V_{SS}. This design permits direct logic-level addressing and writing, and a choice of either logic-level or current-sensing readout. Addressing and sensing can be accomplished with MOS or bipolar transistor circuits. Fig.14(e) shows a typical timing diagram for the COS/MOS memory circuit.

The characteristics of the CD4005 or CD4005D NDRO memory circuit can be summarized as follows:

- Quiescent Power Dissipation
  (All X, Y Inputs and Sense at ground) (V_{DD}=D_0=D_1=10V) . . . . . 10 (typ) mW
- "0" DC Sense Current . . . . . 20 (max) μA
- "1" DC Sense Current . . . . . 500 (min) μA
- DC Input Current (V_{IN}=OV or 10V) . . . . . 1 (typ) nA

(Cont'd)

- Data Input Current (D_o=D_1=X_i=Y_j= 10V) ..... 500 (min) μA

  (D_o or D_1=OV;X_i=X_j=10V) (Pulse Width 50 ns) ..... -1 (typ) mA

- Input Capacitance ..... 15 (max) pF
- Output Capacitance ..... 25 (max) pF
- Sense-Line Capacitance ..... 25 (max) pF
- Sense "1" Read Delay Time (V_{DD}=20V, V_{ss}=OV; C_{out}=30p_F) ..... 25 (max) ns
- Write-Pulse Duration (" , " ; ") ..... 75 (max) ns
- Diode protection at all MOS gate input points

Expansion of 16-Bit NDRO COS/MOS Memory Circuit

Expansion of the NDRO memory beyond the 16-word one-bit capacity can be accomplished easily by use of any number of CD4005 or CD4005D packages. Fig.15 shows how 32 packages can be interconnected to produce a 64-word, 8-bit memory. Word capacity is increased by horizontal expansion in the X and Y directions (increasing the number of cell locations). The sense lines in each plane (each plane represents one bit) are made common, either by direct connection or through gates; similarly, the D_o lines are made common and the D_1 lines are made common in the same manner.

Bit expansion is accomplished by an increase in the number of horizontal planes. The corresponding X and Y terminals in each plane are connected together directly or through gating.

EXAMPLE: To write the binary word 10111011 (least significant bit is bit 1) into word locations 3, 4:

(1) X_3 and Y_4 inputs are set to a high level (H)

(2)

Bit #	D_o	D_1
1	H	L
2	H	L
3	L	H
4	H	L
5	H	L
6	H	L
7	L	H
8	L	H

To read this same word out of word location 3, 4:

(1) X_3 and Y_4 are again set to a high level (H)

(2) Current from an external source is supplied on the D_1 line for each bit (D_1 is set to a high level)

(3) All D_o lines are maintained at a high voltage level

All sense leads associated with cells in which a "1" was stored will carry approximately 500 micro-amperes; those cells containing a "0" will pass virtually zero current through their respective D_1 leads.

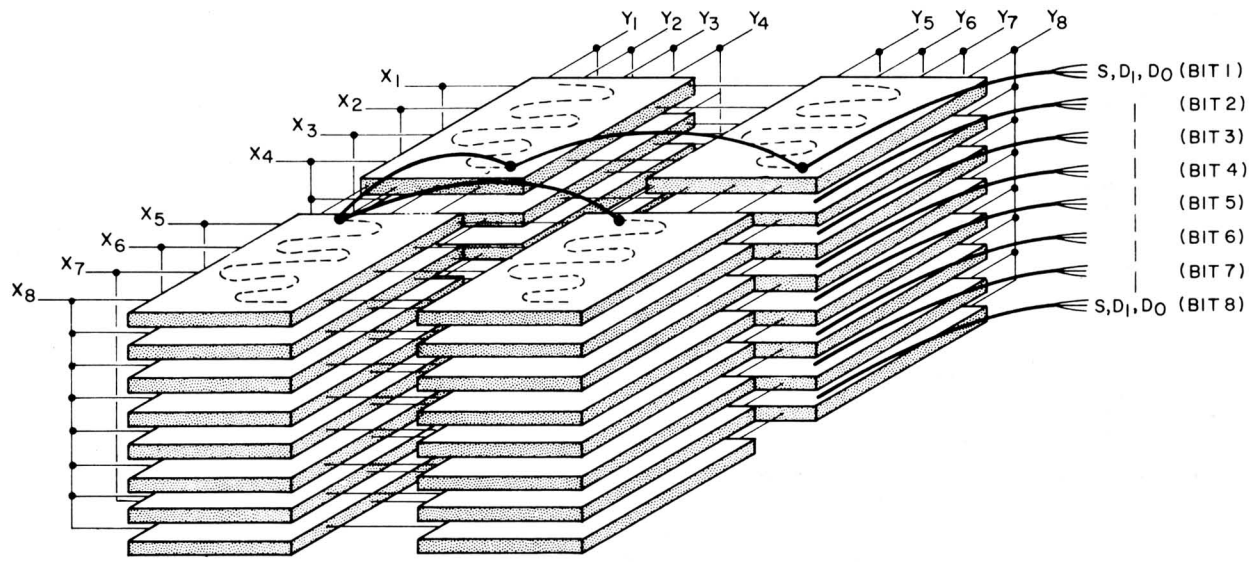


Fig.15 - 64-word, 8-bit memory using 32 arrays of the type shown in Fig.14.

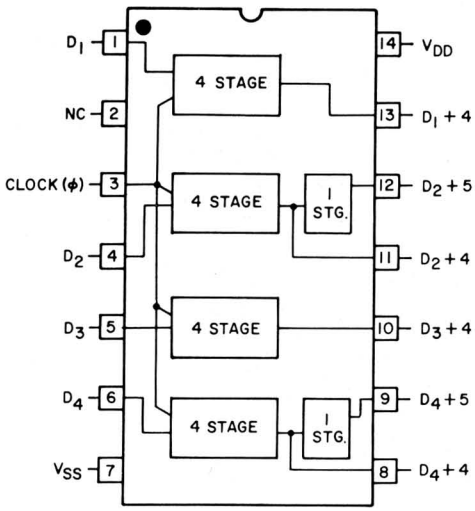
A LOW-POWER COS/MOS 18-STAGE STATIC SHIFT REGISTER
MSI (Medium Scale Integration)

Fig.16 shows several diagrams for an 18-stage static shift register using COS/MOS transistors. The functional diagram in Fig.16(a) shows that the RCA CD4006 or CD4006D is composed of four separate "shift register" sections; two sections contain four stages and each of the other two sections have five stages (4 + 1). Each section has an independent 'data" input and a "Q" output from the fourth stage. This configuration permits easy implementation of various shift-register lengths in the range from 4 to 18 stages. Specifically, multiple-register sections of 4, 5, 8, and 9 stages or single-register sections of 10, 12, 13, 14, 16, 17, and 18 can be implemented by use of one CD4006 or CD4006D package. Longer shift-register sections can be assembled by use of more than one package.

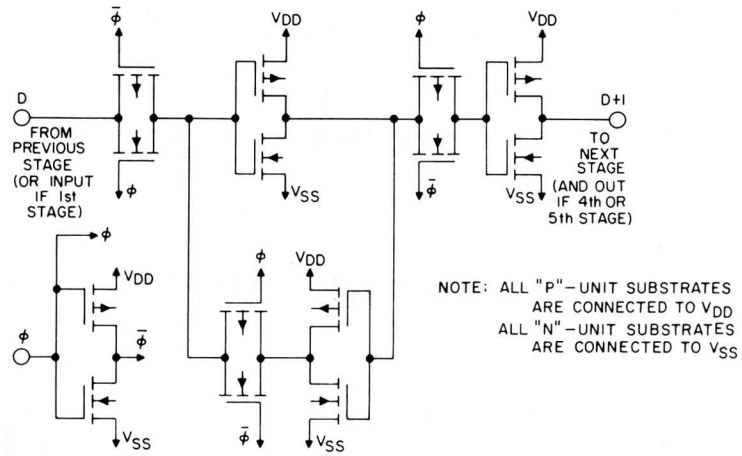
Fig.16(b) shows that a single COS/MOS shift-register stage is in reality a flip-flop coupled at the input and the output by transmission gates. (COS/MOS flip-flops and their associated transmission gates are described in more detail later.)

Mode of Operation

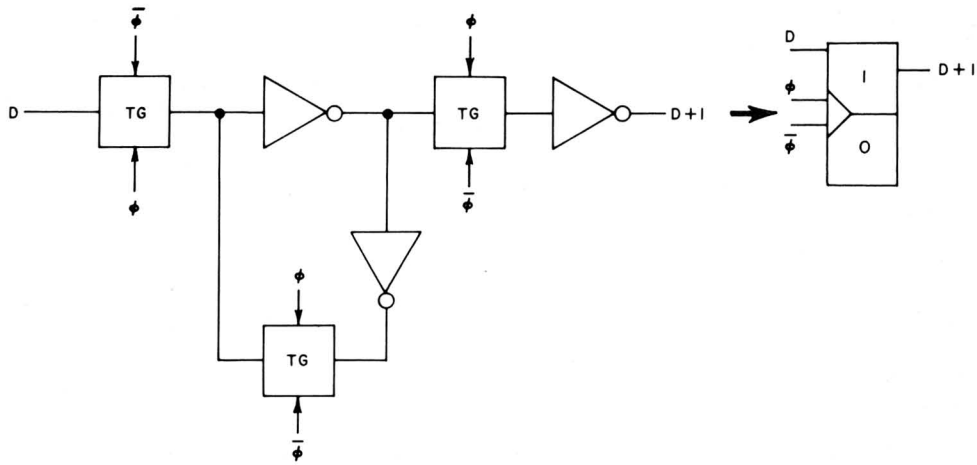
A common clock signal is used for all stages. Information presented at the "D" line of any of the four register sections is shifted into that particular section under the control of the common clock signal. A "1" or "0" logic level at the "D" line during the negative-going transition of the clock signal is transferred into stage 1 of the shift register section, as shown in Fig.16(f). Simultaneously, the information in all of the register stages shifts over one position. The fourth and fifth stages of a register subsequently present the "D" input information, delayed by 4 and 5 clock periods, respectively. Circuit operation is such that permanent register storage exists for a low clock-line state. The clock-line high level, however, should be less than 10 microseconds wide to assure proper register operation.



(a) Functional Diagram



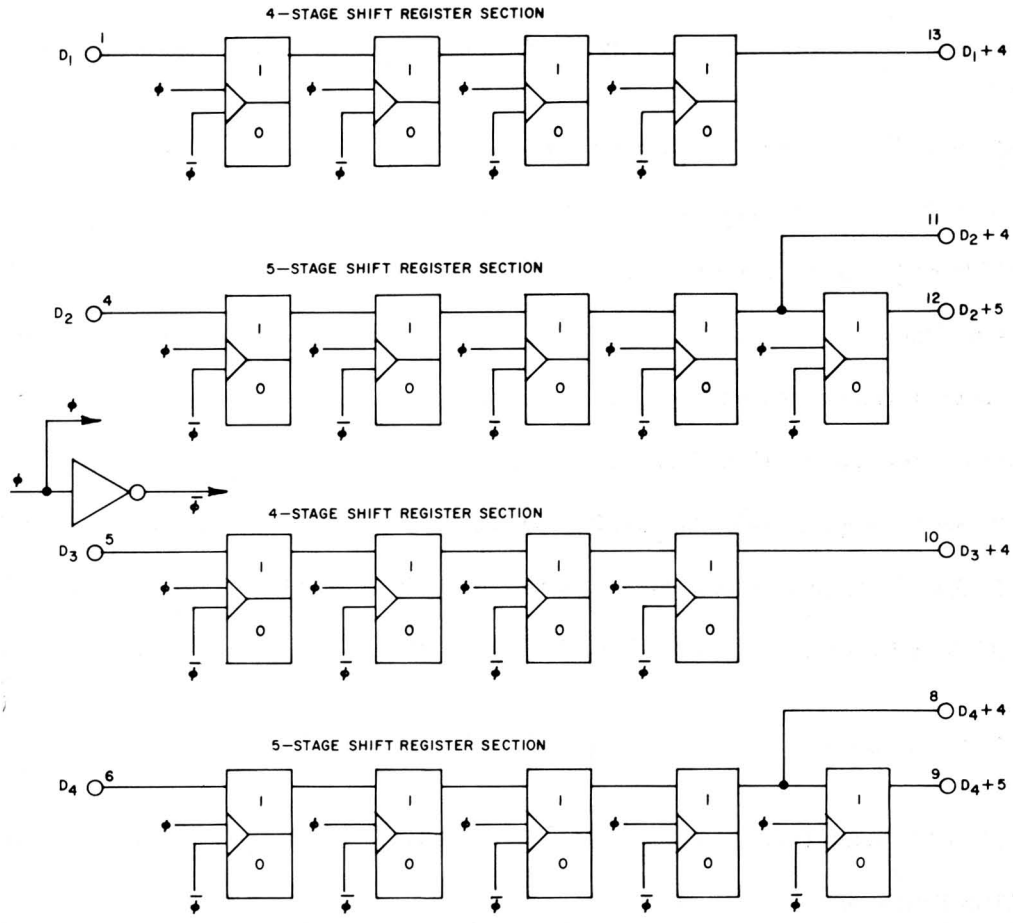
(b) Schematic Diagram of Clock Pulse Shaper and One Shift Register Stage



TG = Transmission Gate Input to Output is:
a) a bidirectional short circuit when control input 1 is "low" and control input 2 is "high"
b) an open circuit when control input 1 is "high" and control input 2 is "low".

(c) Equivalent Logic Diagram and Shorthand Representation for One Shift Register Stage

Fig.16 (Cont'd)

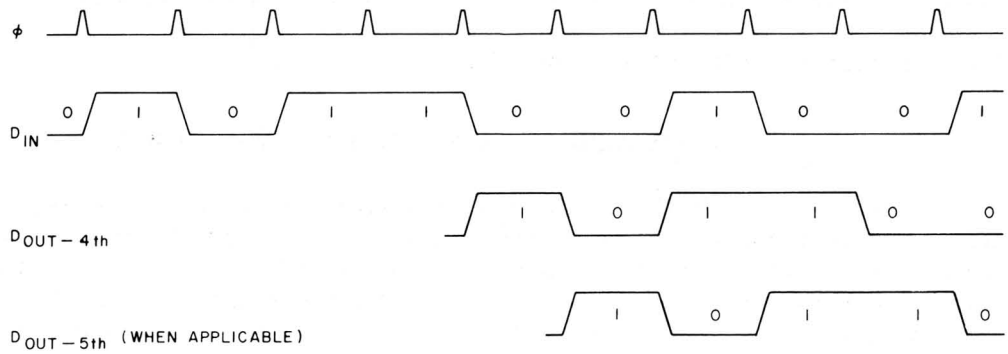


(d) Logic Diagram

D	ϕ▲	D + 1
0	⌐	0
1	⌐	1
X	⌐	NC

NC = No Change;
X = Don't Care;
▲ = Level Change

(e) Truth Table for One Shift Register Stage



(f) Typical Tuning Diagram for One Register Section

Fig.16 - Functional diagram, partial schematic diagram, logic diagrams, truth table, and timing diagram for an 18-stage static shift register using COS/MOS transistors (CD4006 14-lead ceramic flat package; CD4006D 14-lead dual-in-line ceramic package).

The characteristics of the CD4006 or CD4006D 18-stage static shift register can be summarized as follows:

- Quiescent Power Dissipation (V_{DD} = 10V) . . . . . 100 (typ) nW
- DC Input Current on Data Line . . . . . 1 (typ) nA
- DC Input Current on Clock Line . . . . . 10 (typ) nA
- Noise Immunity . . . . . 4 (typ) V
- Input Capacitance for Data Line . . . . . 5 (typ) pF
- Input Capacitance for Clock Line . . . . . 50 (typ) pF
- "0" Shift Propagation Delay (4-Stage Register Section) (C_L = 15 pF) . . . . . 150 (typ) ns
- "1" Shift Propagation Delay (4-Stage Register Section) (C_L = 15 pF) . . . . . 200 (typ) ns
- "0" Clock Duration (" " ")(" ") . . . . . 0.25 (min) μs ∞ (max)
- "1" Clock Duration (" " ")(" ") . . . . . 0.25 (min) μs 10 (max) μs
- "0" or "1" Setup Time (" " ")(" ") . . . . . 250 (min) ns
- Clock-Pulse Rise and Fall Times (" " ")(" ") . . . . . 1 (max) μs
- Clock-Pulse Input Frequency (" " ")(" ") . . . . . 2 (max) MHz
- Large Fan-out . . . . . up to 50
- Shifting Rate . . . . . 1 MHz
- Permanent Register Storage with clock line low - No information recirculation required
- Diode Protection on all COS/MOS Gate Input Points

TRANSMISSION GATES IN COS/MOS CIRCUIT DESIGN

As mentioned previously, COS/MOS circuits have capacitive input; therefore, dc-coupling problems are reduced and capacitive storage action can be used to simplify circuit designs. The transmission gate[1, 2] (also known as a bidirectional gate) of Fig.17 is useful for charging or discharging a capacitive load such as a gate or the output capacitance of another MOS transistor. As shown in Fig.17(a), an MOS transistor can function as a bilateral device, i.e., the functions of source and drain can reverse, so that a reversal of current-flow direction is possible. A transmission gate operates as a drain-loaded stage in one current direction, and as a source-follower in the other direction. The latter type of operation results in slow speed in large-signal applications, and also causes the MOS transistor to shut off when the voltage difference from gate to source equals the threshold voltage. Consequently, premature cutoff can occur as compared to an ideal switch. Both of these problems can be obviated to a considerable degree if the voltage swing at A is larger than the required output (capacitive-load) swing. As an alternate solution, the COS/MOS transmission-gate shown in Fig.17(b) can be

used. In this arrangement, one of the transistors can always operate as a normal drain-loaded stage in either direction. Transmission gates have been used in counters,[3] shift registers[1,4] and memories. Examples of such applications were shown in Figs.13, 14, and 16.

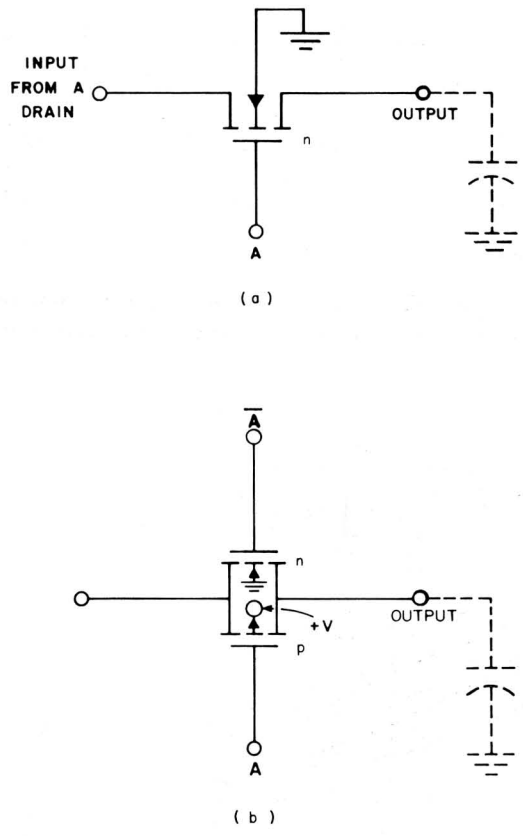
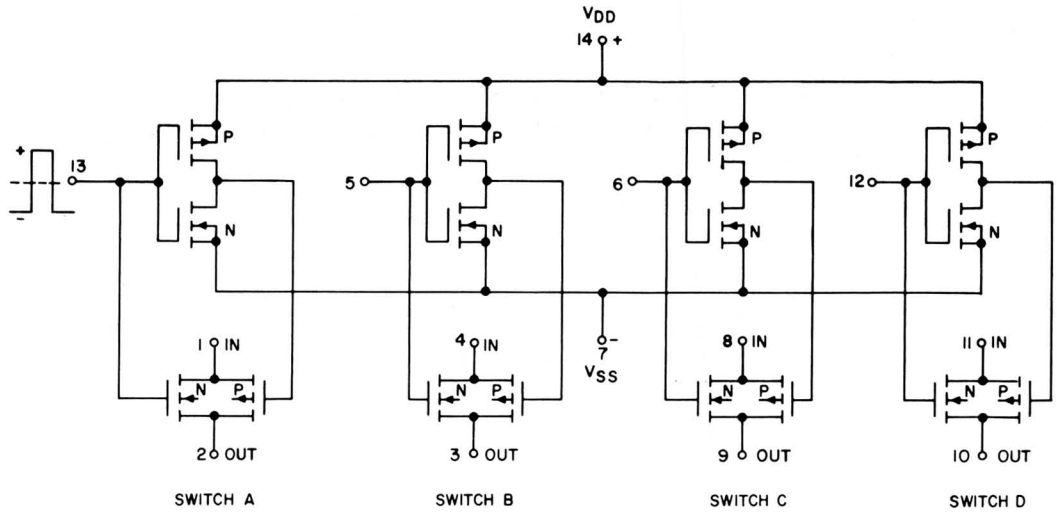


Fig.17 - MOS transmission gates.

A COS/MOS Multiplexer using Transmission Gates

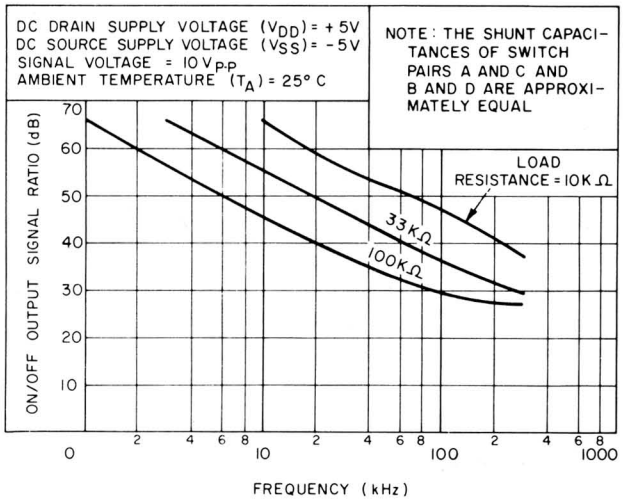
COS/MOS transistors are also applicable to multiplexer circuits for switching analog or digital signals. The principles of operation have been demonstrated in a simple 4-channel multiplexer of monolithic construction (RCA Dev. No. TA5460), shown in Fig.18(a). This circuit contains four independent, bilateral signal switches, each of which is controlled by an external signal (e.g., switch A is controlled by a gating signal applied at terminal 13). Only positive-polarity gating signals are required because internal inverters provide negative signals to actuate the p-channel MOS transistors. The actual signal switching is performed by a COS/MOS type of transmission gate which is interposed between each set of four "In" - "Out" terminals. Fig.18(b) shows the typical on/off output-signal ratios (as a function of signal frequency) which can be achieved in each of the multiplexer switches. At a frequency of 10 kHz and loads of 10000 ohms, the cross-talk between adjacent channels is typically 64 dB.

In multiplexing analog signals, the circuit is operated with two equi-voltage power supplies of opposite polarities. Fig.18(c) shows the maximum peak input signal voltage as a function of the dc supply voltages (with the switching channel in the "OFF" conditions). At a signal frequency of 1 kHz (load of 10000 ohms), the distortion of a sine wave is typically about 1 per cent as a result of transmission through a multiplexer channel. Transfer-characteristic deviation from the closest linear slope is typically 4.7 per cent.

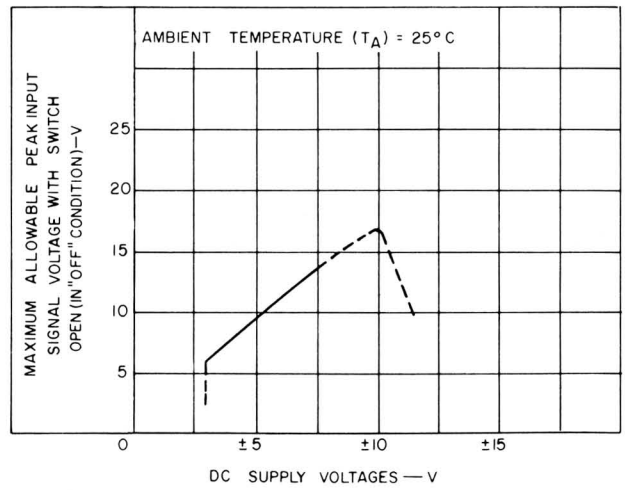


NOTE: All switch p-channel substrates are internally connected to terminal No.14.
All switch n-channel substrates are internally connected to terminal No.7.

(a)



(b)



(c)

Fig.18 - Schematic diagram and characteristics of COS/MOS 4-channel multiplexer for analog or digital signals (RCA Dev. No.TA5460).

The characteristics of the RCA Dev. No. TA5460 4-channel multiplexer can be summarized as follows:

- Supply Voltages

Sine-Wave Operation	(V_{DD}	+8 (max) V
	(V_{SS}	-8 (max) V
Pulsed Operation:	(V_{DD}	+16 (max) V
	(V_{SS}	0 (max)

- Quiescent DC Current Drain . . . . . 100 (typ) nA
- "On" Channel Resistance . . . . . 425 (typ) ohms
- Gate Control Voltage . . . . . +8 (max) V
  (Gate voltage should be approximately V_{DD} for Channel "On" condition or approximately V_{SS} for Channel "Off" condition)
- Signal Voltage (with minimum load resistance of 10000 ohms) . . . . . +7 (max) V
- Output Voltage (R_L = 10000 ohms; V_{IN} = 10 V; V_{DD} = 10 V; V_{SS} = 0) . . . . . 9.5 (typ) V

COS/MOS TRANSISTORS IN SHIFT-REGISTER AND COUNTER DESIGNS

COS/MOS transistors can be used to form a true complementary-logic shift register consisting of two flip-flops per bit for two-phase operation.[5] However, a significant reduction in components can be obtained by the use of the excellent capacitance-storage features of COS/MOS gates. As shown in Fig.19, switches S_1 and S_2 are in series with the cross-coupling connections of the flip-flop. When these switches are open, two separate storage elements are formed, i.e., the left side and the right side of the flip-flop. Each side can store information for an extended (but finite) period of time. Digital information from a "preceding stage" is applied to the gates of the left side, and can thereby change the state of the left side. Simultaneously, the right side can be imparting its information to the left side of the "next stage". If switch S_2 is closed first, followed by S_1, the "1" or "0" information transferred from the preceding bit is locked into the left side.

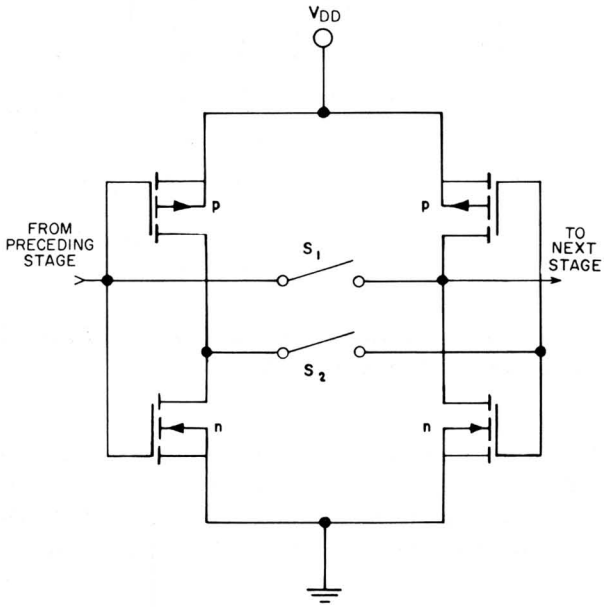


Fig.19 - Shift-register stage.

If the switches S_1 and S_2 in Fig.19 are replaced by MOS devices and appropriate clocking connections, the static shift-register circuit shown in Fig.20 can be derived. Transistor N_5 locks the flip-flop comprising P_1-N_1 and P_2-N_2. However, because information must flow from left to right when N_3 and N_5 conduct, N_5 is designed to conduct much less current than N_3 when equal gate voltages are applied. As a result, the capacitance represented by the gates of P_1-N_1 charges much more slowly than the capacitance of gates P_2-N_2, and information is propagated from left to right. Clock voltage levels can be made equal to logic levels in this circuit.

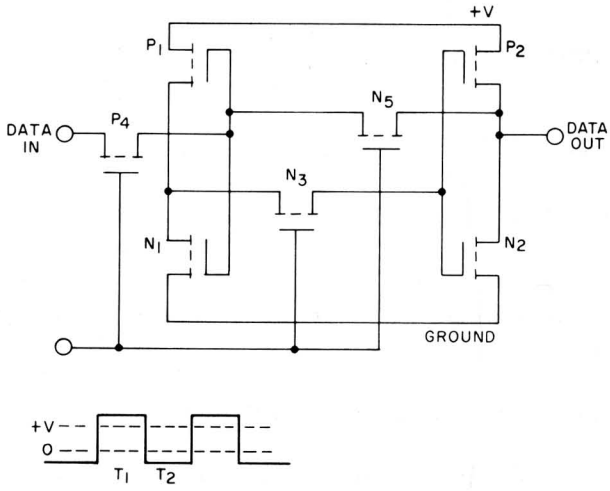


Fig.20 - Static shift-register stage with single transmission gates and single-phase clock.

The dual-transmission-gate[6] version of the circuit in Fig.20 is shown in Fig.21. COS/MOS transistors P_1-N_1 and P_2-N_2 comprise the flip-flop; the COS/MOS transmission gates P_3-N_3 and P_5-N_5 are analogous to the switches S_1 and S_2 of Fig.20. Another transmission gate, P_4-N_4, provides clock-controlled data input. The COS/MOS inverter, P_7-N_7, provides a phase reversal of the clock signal to actuate the appropriate sections of the transmission gates in the circuit.

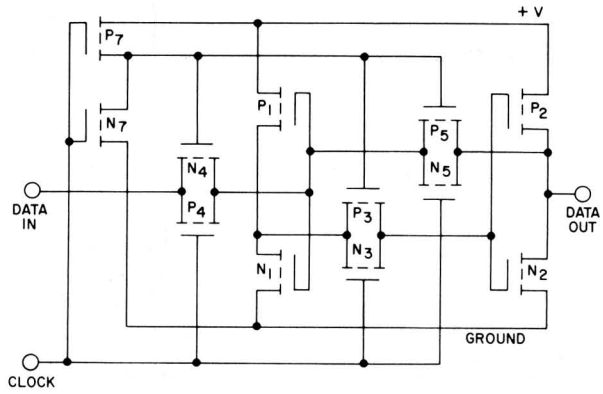


Fig.21 - Static shift-register stage with dual transmission gates and single-phase clock.

The circuit of Fig.22 uses two gate-controlled flip-flops. Information is gated into the flip-flops through a transmission gate, P_5-N_5 or P_8-N_8, and is locked by the action of P_6-N_6 or P_7-N_7. This circuit can be used as a binary counter if the inverted data output is converted to a data input; the clock line then becomes the binary input. Forms of these circuits are used in the COS/MOS flip-flop circuit (Fig.12) and the COS/MOS counter circuit (Fig.13).

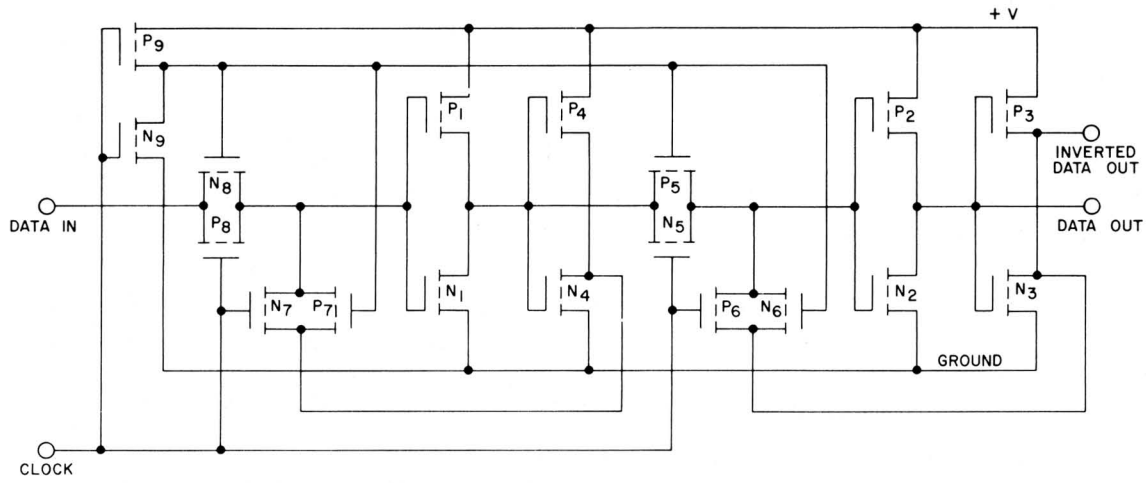


Fig.22 - Static shift-register stage with dual transmission gates and single-phase clock.

COS/MOS TECHNOLOGY AND LARGE-SCALE INTEGRATION (LSI)

The practicality of COS/MOS technology in Medium-Scale Integration (MSI) has been brought to commercial fruition in the circuits shown in Fig.13, 14, and 16. COS/MOS technology also shows great potential for use in LSI because it offers the following features:

- The relatively small chip area consumed by MOS transistors and the elimination of area-consuming resistors result in high circuit density per unit of silicon area.
- The low quiescent power consumption makes it feasible to design comparatively complex arrays on a single chip without encountering restrictions due to power dissipation.
- COS/MOS circuits are suitable for operation over the military temperature range of -55^{o} to $+125^{o}C$; furthermore, the inherent symmetry of the COS/MOS configuration minimizes parameter variations as a function of temperature because there is a degree of inherent temperature compensation.
- COS/MOS technology permits the use of simple "tunnel interconnections" in complex arrays; the design of equivalent complexity in a bipolar LSI array frequently requires the use of "multilayer metalization" interconnections with additional processing steps and their attendant costs.
- COS/MOS circuits have high noise immunity.
- The circuits can operate from single power supplies, of positive or negative polarity, over a wide range of unregulated supply voltages.
- Operation is reliable despite wide variations in transistor characteristics.
- COS/MOS transistors can easily be paralleled for size variations.
- Simple circuits can be designed for single-phase clock operation in the range from dc to frequencies of several megahertz.
- Fixed logic-level swings are relatively independent of system tolerances and fanout.
- Significant reductions in power consumption can provide solutions to heat-dissipation problems in compact design and/or promote the conversion of line-connected equipment to portable, battery-operated versions.
- The available technology is capable of economically reproducing stable COS/MOS units.
- COS/MOS transistors do not require the use of biasing networks.
- Logic-function realization is simplified.

Significant research and advanced-development engineering explorations are being made into the feasibility of the COS/MOS technology for LSI. The scope of these undertakings is indicative of the promise electronics scientists hold for the future potentialities of COS/MOS in LSI. Some typical projects which have been reported are as follows:

(1) Hanchett et al[7] have designed and built experimental 8-word by 9-digit monolithic memory arrays, fabricated entirely with COS/MOS transistors on an 81-by-103-mil silicon pellet. The complete 72-bit array consists of 432 MOS transistors and is mounted in a 28-lead flat package. These arrays have typical write-in times of 40 nanoseconds and read-out times of 30 nanoseconds. The quiescent power dissipation is less than 20 microwatts with a single supply voltage of 10 volts.

(2) Hanchett et al[7] have reported on their progress in designing a 288-bit COS/MOS memory-system array (16 words by 18 digits), shown in Fig.23. The memory is word-organized and non-destructively sensed. Although word organization makes decoding and word-drive circuits more complex, it simplifies the memory cell and, because the number of memory cells is greater than the number of decoder and word-drive circuits, minimizes over-all pellet size. The array consists of a 16-output address decoder, 16 word drivers (which also select either the read or write mode of operation), and 288 memory cells. Eight address inputs are required for a high-speed 16-word MOS address decoder when an X-Y select type of configuration is used, and a read/write signal is necessary for the activation of the word-drive circuits. Information is written into, and read out of, 18 common digit (input-output) lines to minimize external connections to the chip. The memory operates with a single power supply. The 288-bit array, consisting of approximately 1850 devices, can be fabricated on a single silicon chip 155 mils by 175 mils for mounting in a 30-terminal package. Large memory systems can be constructed through the use of multiplicities of these array packages.

(3) Feryszka et al[8] have reported the design of a BCD-to-16-output decoder in COS/MOS configuration. This decoder is effectively the equivalent of 16 four-input NAND gates on one chip. Rise times as low as 50 nanoseconds have been measured, with fall times as low as 20 nanoseconds at each output into a 7-picofarad capacitor.

(4) Ahrons[6] has shown the photomicrograph of a developmental 64-bit COS/MOS static shift register with dual transmission gates and parallel reset, the design work being credited to R. Feryszka and A. Yung. Ahrons also expressed the opinion that "a 500-bit shift register can be made in COS/MOS form with only five pins, one each for supply voltage, ground, input, output, and clock. At a count of four gates per bit, the 500-bit shift register has a gate-to-pin ratio of 400 to 1."

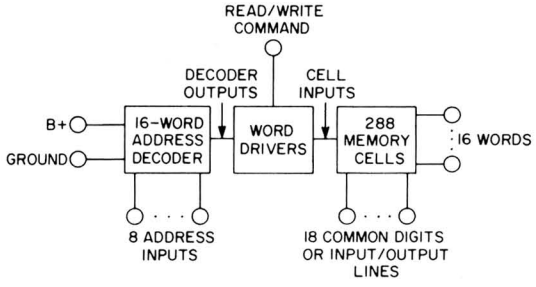


Fig.23 - Block diagram of a 288-bit COS/MOS memory array.

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