November 10, 1963

CHARACTERISTICS OF UNIPOLAR FIELD-EFFECT TRANSISTORS

A diffused-channel, diffused-gate UNIFET structure and its d-c and small signal a-c characteristics will be discussed. The unipolar field-effect transistor may have either an n-type channel or a p-type channel. From a circuit point of view, the structures are the same except that the terminal voltages and currents are of opposite polarities. This discussion will be limited to the p-channel structure.

In Fig. 1, the p-channel device is comprised of a p-type region diffused into an n-type substrate. Subsequently, an n-type gate is diffused into the p-type region leaving a relatively thin channel. The important channel dimensions are its effective thickness T, length L and width W. These dimensions have a direct bearing upon the electrical characteristics of the UNIFET. Under conditions of zero applied voltages, the conductance of the channel is given by:

$$G_0 = \sigma_a \frac{WT}{L}$$

where σ_a = average conductivity of channel.

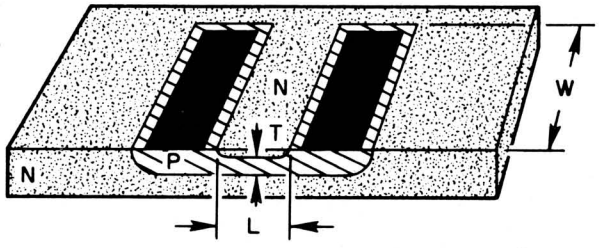

Figure 1

As shown in Fig. 1, the thickness T is the distance between two "transition regions" which exist at the p-n junctions. At the transition regions, there is a "depletion layer" void of free mobile carriers. The depletion layer width can be increased by using a reverse bias

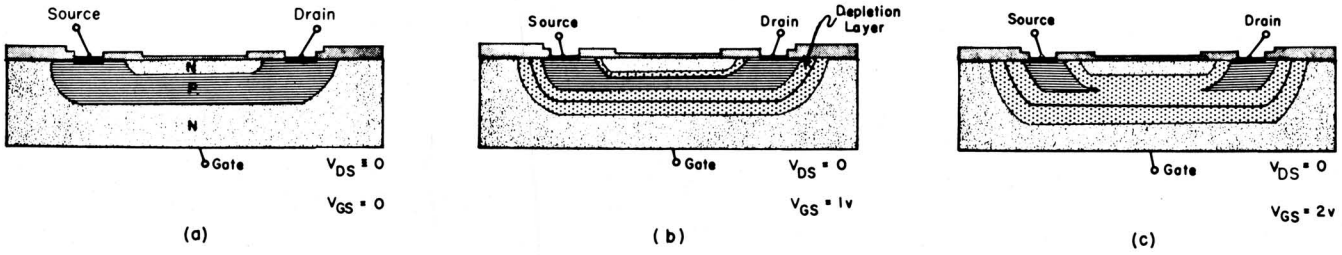

Figure 2

Printed in ELECTRONIC INDUSTRIES, March 1963

across the p-n junction (i.e., positive gate voltage). This decreases the effective channel thickness T, as shown in Fig. 2, and results in a reduction in channel conductance G. Figure 3 shows channel conductance as a function of gate-to-source voltage V_{GS}. If the initial channel thickness T is small enough, the depletion layer will extend deep enough to "pinch off" the channel, as shown in Fig. 2(c), and reduce G to almost zero. The gate-to-source voltage needed to do this is called the "pinch off voltage" shown in Fig. 3 by the symbol V_P.

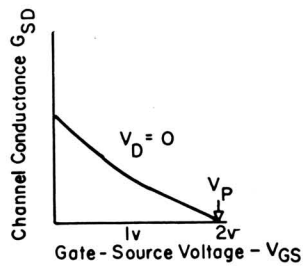

Figure 3

If the gate-to-source voltage is kept at zero and the drain-to-source voltage is made negative, the channel will assume a wedge shape as shown in Fig. 4(a). This is merely the result of a wider depletion layer at the drain end of the channel. Fig. 4(b) shows the result of an increase in drain-to-source voltage V_{DS} to a value about equal in magnitude to V_P, hence the two depletion layers just meet.

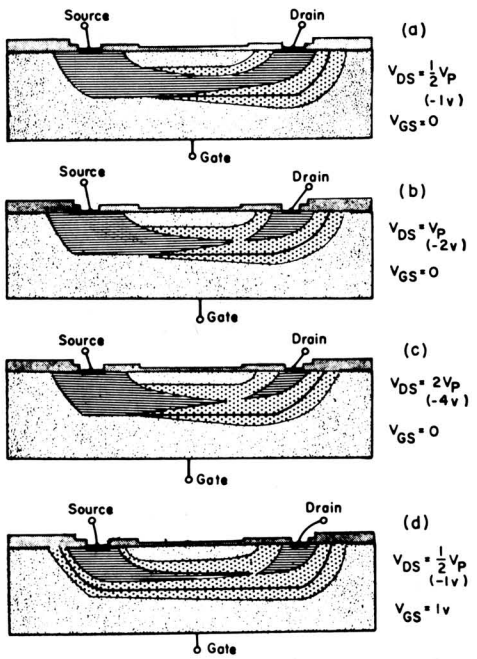

Figure 4

At this point, the incremental impedance of the channel becomes quite high. At higher voltages, as shown in Fig. 4(c), there is little change in the channel shape, but the depletion layers extend further into the drain region. In Fig. 4(d), V_{GS} equals one-half V_P and V_{DS} equals one-half V_P. Since V_{GS} is positive and V_{DS} is negative, the gate-to-drain voltage equals V_P, hence the drain end of the channel is just pinched off as in Fig. 4(c).

Figure 5 shows the I_D vs V_{DS} characteristic curve. Notice that at a drain voltage about equal to the magnitude of V_P, the drain current becomes nearly saturated. This is called the drain-saturation current and is shown in Fig. 5 by the symbol I_{DSS}.

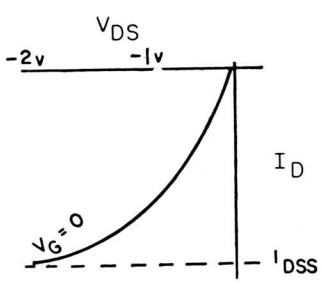

Figure 5

Avalanche Breakdown

As the drain voltage increases, the electric field in the depletion layer increases until "avalanche breakdown" occurs. Beyond this voltage, the drain-to-gate current increases very rapidly. Note that this is a drain-to-gate breakdown, not a drain-to-source breakdown.

In the most common mode of operation, the gate is kept in the zero or reverse-bias condition. That is, for the p-channel device, V_{GS} will be zero or positive, and V_{DS} will be negative. Figure 6 shows the static characteristics of a p-channel UNIFET. Figure 6(a) presents the drain current I_D as a function of V_{DS} for constant values of V_{GS}. These curves show that the saturated value of drain current is a function of V_{GS}. The value for $V_{GS} = 0$ is I_{DSS} as was shown also in Fig. 5.

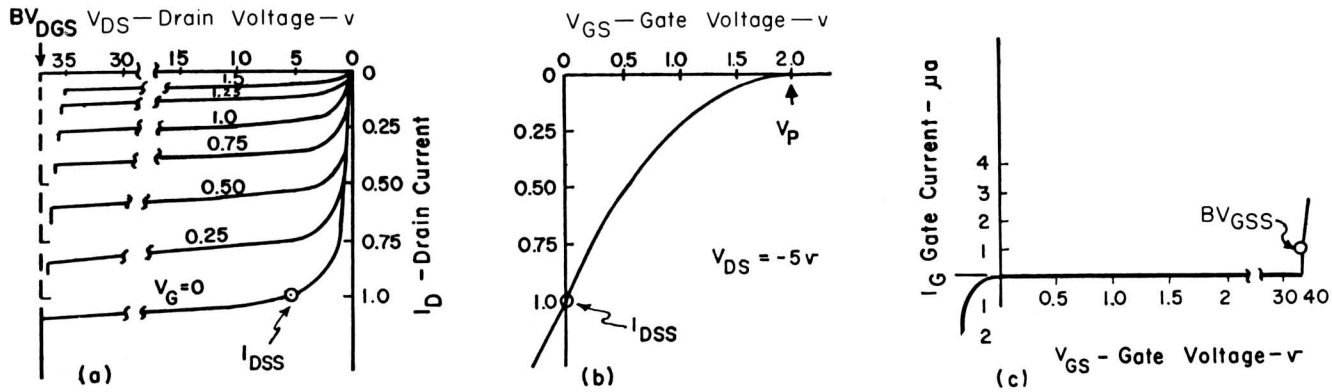

Fig. 6 (a) I_D as a function of V_{DS} (b) Gate-voltage drain-current characteristic (c) gate-current gate-voltage characteristic

Figure 6(b) shows the gate-voltage drain-current transfer characteristic for constant values of drain voltage V_{DS}. These curves are a different way of presenting the data contained in Fig. 6(a). Note the similarity of these I_D vs V_{GS} characteristics to the G_{SD} vs V_{GS} curve of Fig. 3. Figure 6(c) shows the gate-current gate-voltage characteristic. This curve shows that the dynamic conductance of the gate is very low in the region between $V_{GS} = 0$ and $V_{GS} = BV_{GSS}$. The gate current I_{GSS} in this region may range from 10^{-10} to 10^{-8} amps, depending on the size of the device.

The UNIFET d-c characteristics could be given by graphs as was done in Fig. 6; however, it is better to use static parameters of which I_{DSS}, V_P, I_{GSS} and BV_{GSS} are the most useful.

Common-Source Configuration

For linear small-signal operation, the UNIFET will be biased to an operating point. For general applications, the common-source configuration is probably the most useful. An a-c input signal will be applied to the gate and an output signal taken from the drain with the source being common to the input and output. Thus the UNIFET can be considered as a three-terminal network characterized by four small-signal a-c parameters. Because of the nature of its characteristics, i.e., high input and output impedances, use of the admittance

parameters is recommended. They are defined by the equations:

$$i_i = y_{is} v_{gs} + y_{rs} v_{ds}$$

$$i_o = y_{fs} v_{gs} + y_{os} v_{ds}$$

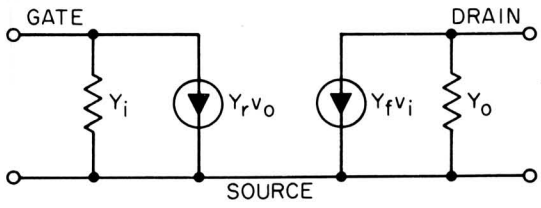

Figure 7

The two-generator equivalent circuit based on the use of these parameters is shown in Fig. 7.

Values of the small-signal parameters in the equivalent circuit may be found with a conventional admittance bridge. They are a function of the bias voltages and currents as shown in the curves of Fig. 6. For example, the small-signal output conductance g_{os} decreases as V_{DS} is increased. Principal capacitance associated with UNIFETs is depletion-layer capacitance. Since the depletion layer widths are a function of voltage, the capacitances are voltage sensitive. Transconductance g_{fs} is a measure of the effect of gate voltage upon drain current. Its magnitude is a function of drain current.

One problem facing the circuits designer is that of obtaining enough data on a new device to use it to its full potential. Parameters selected by the manufacturer often are not coordinated with user needs. A small-signal parameter value at unlikely bias conditions may be of little value. Gate capacitance of field-effect transistors, for example, may be minimized by increasing V_{GS}. This can result in a gate capacitance specification that looks good on a data sheet, but if the value of V_{GS} exceeds pinch-off voltage, this would be an unlikely bias condition for an amplifier.

What are the small-signal data needed by the circuits designer? Under what bias conditions should these data be obtained? How should parameter variations or spread be expressed? On what parameters should minimum or maximum limits be applied? The answers to these questions are important to both the circuits designer and the manufacturer.

By the careful choice of a relatively few static and small-signal parameters specified as control parameters, and by giving information concerning the distribution and interrelation of "controlled" and "uncontrolled" parameters, a manufacturer can provide the data needed for many applications. The static parameters shown on the curves of Fig. 6 represent a reasonable set of "controlled" static parameters. When values for these parameters and small-signal parameters are specified on a data sheet, test conditions should also be given.

Printed in USA